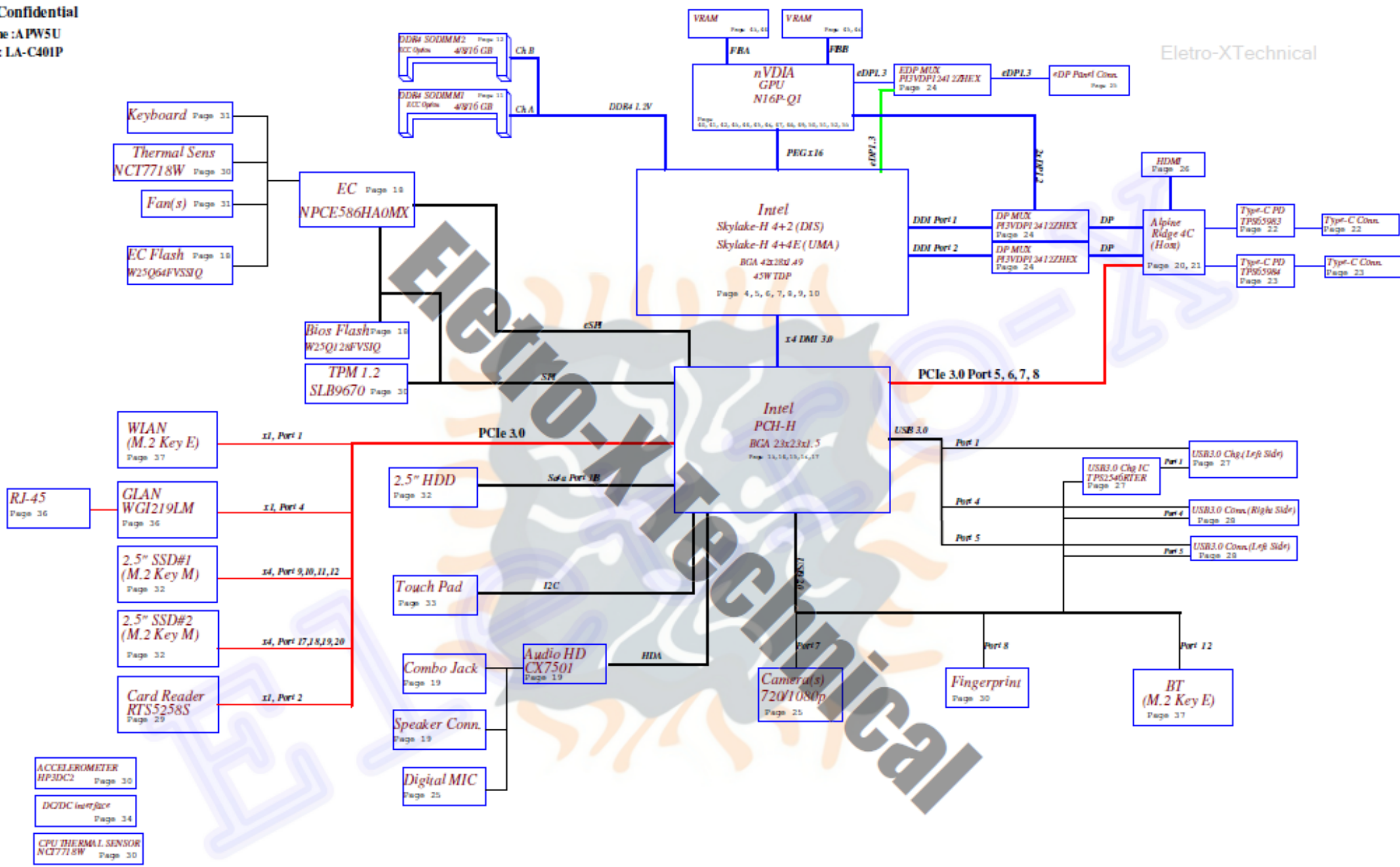


COMPAL CONFIDENTIAL

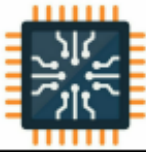
**INTEL SKYLAKE-H PROCESSOR WITH SPT-H_PCH
GPU N16P-Q1-A2**

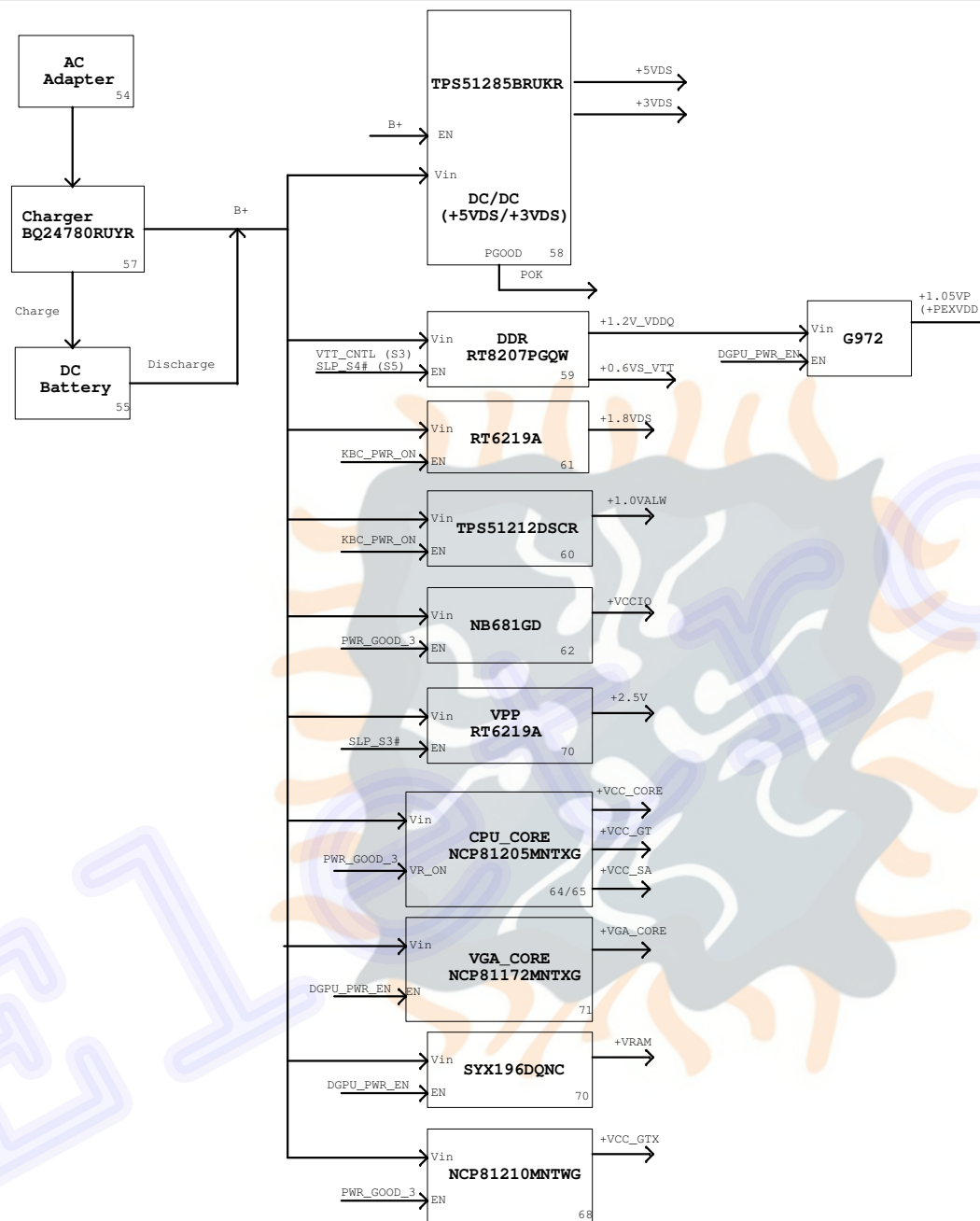
APW5U LA-C401P

2015-11-19 REV 1.



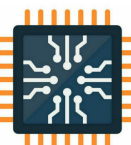
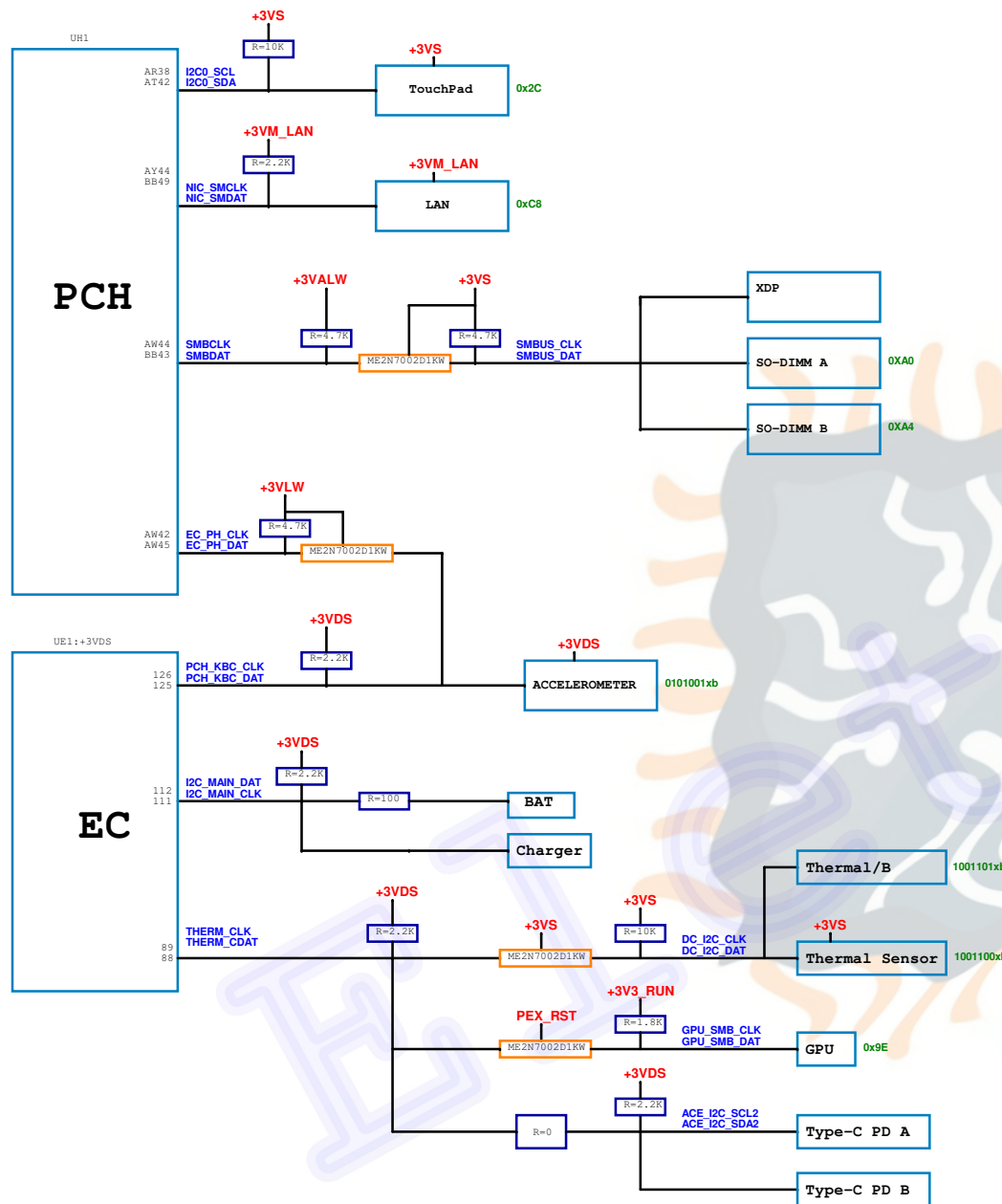
Block Diagrams		LA-C401P	
Block Diagrams		LA-C401P	





CPU DC/DC NCP81205MNTXG ?	
INPUTS	OUTPUTS
B+	+VCC_VORE +VCC_GT +VCC_SA
CPU DC/DC NCP81210MNTWG ?	
INPUTS	OUTPUTS
B+	+VCC_GTX
VGA DC/DC NCP81172MNTXG ?	
INPUTS	OUTPUTS
B+	+VGA_CORE
VRAM DC/DC SYX196DQNC ?	
INPUTS	OUTPUTS
B+	+VRAM
SYSTEM DC/DC TPS51285BRUKR ?	
INPUTS	OUTPUTS
B+	+3VDS/5VDS
SYSTEM DC/DC RT8207PGQW ?	
INPUTS	OUTPUTS
B+	+1.2V_VDDQ +0.6VS_VTT
SYSTEM DC/DC RT6219A ?	
INPUTS	OUTPUTS
B+	+1.8VDS
SYSTEM DC/DC TPS51212DSCR ?	
INPUTS	OUTPUTS
B+	+1.0VALW
SYSTEM DC/DC NB681GD ?	
INPUTS	OUTPUTS
B+	+VCCIO
SYSTEM DC/DC RT6219A ?	
INPUTS	OUTPUTS
B+	+2.5V
CHARGER BQ24780RUYR ?	
INPUTS	OUTPUTS
VIN BATT	B+
SYSTEM LDO G972	
INPUTS	OUTPUTS
+1.2V_VDDQ	+1.05VP (+PEXVDD)
Switches ?	
INPUTS	OUTPUTS





Voltage Rails (O MEANS ON X MEANS OFF)

power plane	+RTCVCC	B+	+5VDS +3VDS +1.8VALW +1VALW	+1.2V_VDDQ +1.0V_VCCST +2.5V	+5VS +3VS +0.6VS_VTT +VCC_IO +VCC_GTX +VCC_CORE +VCC_GT +VCC_SA	
State						
S0	O	O	O	O	O	
S3	O	O	O	O	X	
S5 S4/AC	O	O	O	X	X	
S5 S4/ Battery only	O	O	X	X	X	
S5 S4/AC & Battery don't exist	O	X	X	X	X	

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

CONN@ : means ME part.

Layout Notes

07/24 update

 : Question Area Mark.(Wait check)

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

ROYALTY@ : HDMI LOGO means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.1

EMI@ : means just build for EMI's part

ESD@ : means just build for ESD's part

RF@ : means just build for RF's part

LPC@ : means just build for LPC for EC

ESPI@ : means just build for eSPI for EC

HDD@ : means just build for HDD(option)

SSD@ : means just build for SSD (option)

H42@ : pop on CPU H42 sku only

H44e@ : pop on CPU H44e sku only

DIS@ : pop on DGPU sku only

UMA@ : pop on UMA sku only

DB@ : means just build for Debug port part Remove before MP

SMBUS Control Table

	SOURCE	BATT	Therm Sensor 1001100xb MB side	G-SENSOR 0101001xb	N16P 0x9E	NIC 0xC8	XDP	SODIMM 0XA0 0XA4	TP 0x2C	Therm Sensor 1001101xb DB side
I2C_MAIN_CLK I2C_MAIN_DAT	NPCE586	V	X	X	X	X	X	X	X	X
THERM_CLK THERM_DAT	NPCE586	X	V	X	V	X	X	X	X	V
PCH_KBC_CLK PCH_KBC_DATA	NPCE586	X	X	V	X	X	X	X	X	X
NIC_SMCCLK NIC_SMDAT	Skylake	X	X	X	X	V	X	X	X	X
SMBUS_CLK SMBUS_DAT	Skylake	X	X	X	X	X	V	V	X	X
I2C0_SCL I2C0_SDA	Skylake	X	X	X	X	X	X	X	V	X

USB2.0 Port Table

USB2.0 Port	DESTINATION
1	USB2.0 (MB_Charge)
2	X
3	X
4	USB2.0 (MB_Left Side)
5	USB2.0 (MB_Right Side)
6	X
7	Camera
8	Finger printer
9	X
10	X
11	X
12	WLAN/BT
13	X
14	X

CLKOUT_PCIE Port Table

CLKOUT_PCIE	DESTINATION
0	SSD1
1	VGA
2	LAN
3	WLAN
4	Card Reader
5	Thunderbolt
6	SSD2
7	X
8	X
9	X
10	X
11	X
12	X
13	X
14	X
15	X

HSIO Port Table

Lane#	PCIE	SATA	USB3.0	DESTINATION
1			1	USB3.0(Charger)
2			2	X
3			3	X
4			4	USB3.0 (MB_Left Side)
5			5	USB3.0 (MB_Right Side)
6			6	X
7	1		7	WLAN
8	2		8	Card Reader(PCI-E)
9	3		9	X
10	4		10	LAN
11	5			Thunderbolt
12	6			
13	7			
14	8			
15	9	0A		SSD1 (SATA_SSD or PCIe4 SSD)
16	10	1A		
17	11			
18	12			
19	13	0B		X
20	14	1B		HDD1
21	15	2		X
22	16	3		X
23	17	4		SSD2 (SATA_SSD or PCIe4 SSD)
24	18	5		
25	19			
26	20			

Stapping Options Flash

GPIO 51 Bit 1	GPIO 19 Bit 0	Boot BIOS Destination
0	0	Reserved
0	1	RSVD
1	0	SPI
1	1	LPC

Stapping Options PLT_ID

PLT_ID0	PLT_ID1	PLT_ID2	SKU
0	0	0	
0	0	1	
0	1	0	
0	1	1	17W
1	0	0	
1	0	1	15W
1	1	0	
1	1	1	15U

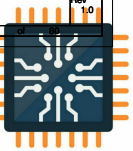
CFG for AR HDMI SET

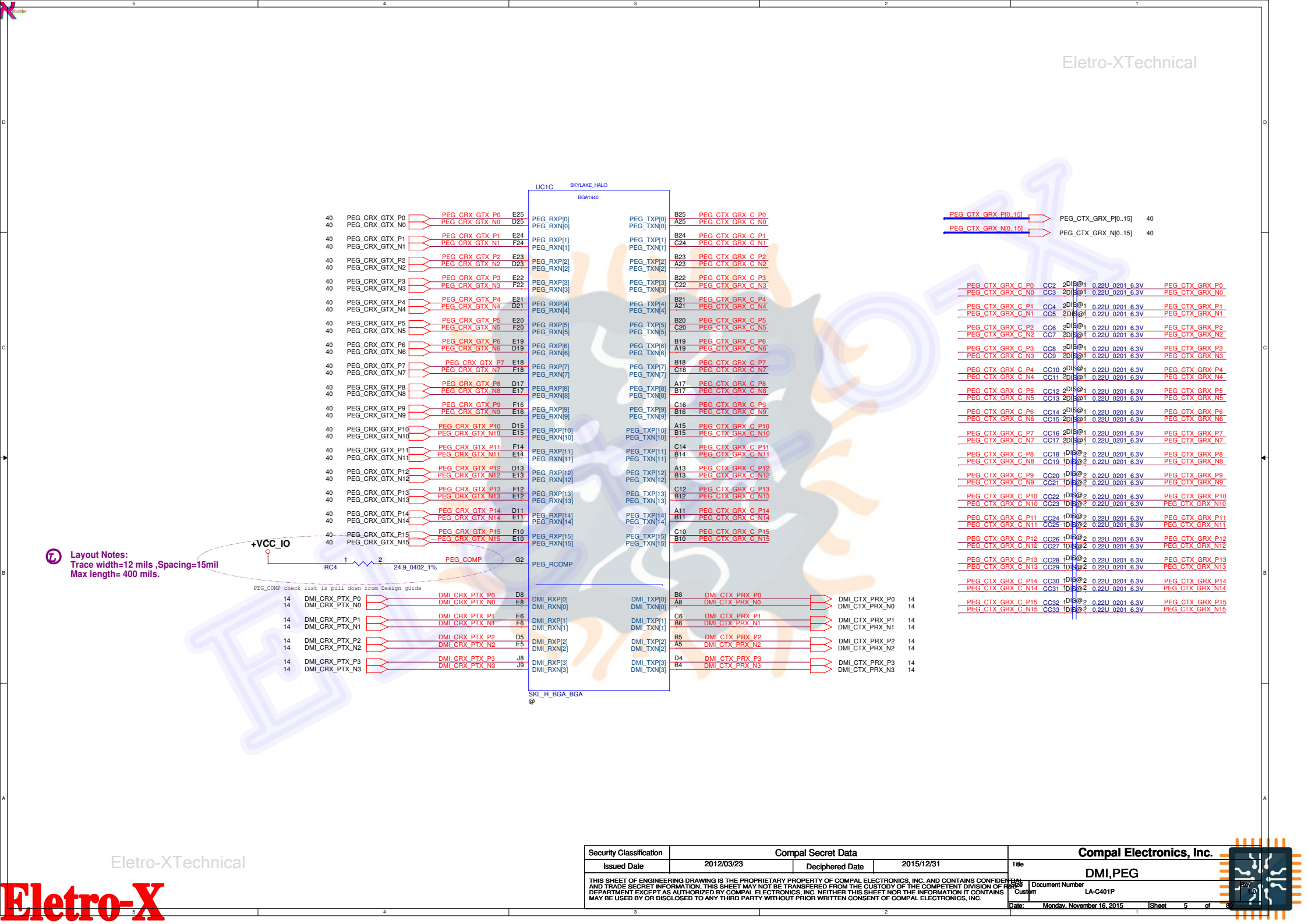
TBT_SRC_CFG1	HIGH	HDMI MODE
--------------	------	-----------

LPC/ESPI Options Resistor

RH198	RH292	RH263	RH282	RH36	RH275	RH117	RH243	RH165	RH168	LE1	LE2	RE85	RE90	RE113	RE110	RH109	RE112	RE39	RE115	RE114	RE89	MODE
V	X	V	V	V	V	V	V	V	X	V	X	V	V	V	V	X	X	X	X	X	X	LPC
X	V	X	X	X	X	X	X	X	V	X	V	X	X	X	X	V	V	V	V	V	V	ESPI

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/03/23	Deciphered Date	2015/12/31	Title	Note List	
Size	C	Document Number	LA-C401P	Rev	1.0	
Date	Monday, November 16, 2015	Sheet	3	of	80	



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Eletro-XTechnical

UC1C SKYLAKE_HALO BGA1440

PEG_CRX_GTX_P0 PEG_CRX_GTX_N0 PEG_CRX_GTX_P1 PEG_CRX_GTX_N1 PEG_CRX_GTX_P2 PEG_CRX_GTX_N2 PEG_CRX_GTX_P3 PEG_CRX_GTX_N3 PEG_CRX_GTX_P4 PEG_CRX_GTX_N4 PEG_CRX_GTX_P5 PEG_CRX_GTX_N5 PEG_CRX_GTX_P6 PEG_CRX_GTX_N6 PEG_CRX_GTX_P7 PEG_CRX_GTX_N7 PEG_CRX_GTX_P8 PEG_CRX_GTX_N8 PEG_CRX_GTX_P9 PEG_CRX_GTX_N9 PEG_CRX_GTX_P10 PEG_CRX_GTX_N10 PEG_CRX_GTX_P11 PEG_CRX_GTX_N11 PEG_CRX_GTX_P12 PEG_CRX_GTX_N12 PEG_CRX_GTX_P13 PEG_CRX_GTX_N13 PEG_CRX_GTX_P14 PEG_CRX_GTX_N14 PEG_CRX_GTX_P15 PEG_CRX_GTX_N15

PEG_RXP[0] PEG_RXN[0] PEG_RXP[1] PEG_RXN[1] PEG_RXP[2] PEG_RXN[2] PEG_RXP[3] PEG_RXN[3] PEG_RXP[4] PEG_RXN[4] PEG_RXP[5] PEG_RXN[5] PEG_RXP[6] PEG_RXN[6] PEG_RXP[7] PEG_RXN[7] PEG_RXP[8] PEG_RXN[8] PEG_RXP[9] PEG_RXN[9] PEG_RXP[10] PEG_RXN[10] PEG_RXP[11] PEG_RXN[11] PEG_RXP[12] PEG_RXN[12] PEG_RXP[13] PEG_RXN[13] PEG_RXP[14] PEG_RXN[14] PEG_RXP[15] PEG_RXN[15]

PEG_TXP[0] PEG_TXN[0] PEG_TXP[1] PEG_TXN[1] PEG_TXP[2] PEG_TXN[2] PEG_TXP[3] PEG_TXN[3] PEG_TXP[4] PEG_TXN[4] PEG_TXP[5] PEG_TXN[5] PEG_TXP[6] PEG_TXN[6] PEG_TXP[7] PEG_TXN[7] PEG_TXP[8] PEG_TXN[8] PEG_TXP[9] PEG_TXN[9] PEG_TXP[10] PEG_TXN[10] PEG_TXP[11] PEG_TXN[11] PEG_TXP[12] PEG_TXN[12] PEG_TXP[13] PEG_TXN[13] PEG_TXP[14] PEG_TXN[14] PEG_TXP[15] PEG_TXN[15]

B25 A25 B24 C24 B23 A23 B22 C22 B21 A21 B20 C20 B19 A19 B18 C18 B17 A17 B16 C16 B15 A15 B14 C14 B13 A13 B12 C12 B11 A11 B10 C10 B09 A09 B08 C08 B07 A07 B06 C06 B05 A05 B04 C04 B03 A03 B02 C02 B01 A01 B00 C00

PEG_CTX_GRX_C_P0 PEG_CTX_GRX_C_N0 PEG_CTX_GRX_C_P1 PEG_CTX_GRX_C_N1 PEG_CTX_GRX_C_P2 PEG_CTX_GRX_C_N2 PEG_CTX_GRX_C_P3 PEG_CTX_GRX_C_N3 PEG_CTX_GRX_C_P4 PEG_CTX_GRX_C_N4 PEG_CTX_GRX_C_P5 PEG_CTX_GRX_C_N5 PEG_CTX_GRX_C_P6 PEG_CTX_GRX_C_N6 PEG_CTX_GRX_C_P7 PEG_CTX_GRX_C_N7 PEG_CTX_GRX_C_P8 PEG_CTX_GRX_C_N8 PEG_CTX_GRX_C_P9 PEG_CTX_GRX_C_N9 PEG_CTX_GRX_C_P10 PEG_CTX_GRX_C_N10 PEG_CTX_GRX_C_P11 PEG_CTX_GRX_C_N11 PEG_CTX_GRX_C_P12 PEG_CTX_GRX_C_N12 PEG_CTX_GRX_C_P13 PEG_CTX_GRX_C_N13 PEG_CTX_GRX_C_P14 PEG_CTX_GRX_C_N14 PEG_CTX_GRX_C_P15 PEG_CTX_GRX_C_N15

CC2 CC3 CC4 CC5 CC6 CC7 CC8 CC9 CC10 CC11 CC12 CC13 CC14 CC15 CC16 CC17 CC18 CC19 CC20 CC21 CC22 CC23 CC24 CC25 CC26 CC27 CC28 CC29 CC30 CC31 CC32 CC33

PEG_CTX_GRX_P0_15 PEG_CTX_GRX_N0_15

PEG_COMP check list is pull down from Design guide

DML_CRX_PTX_P0 DML_CRX_PTX_N0 DML_CRX_PTX_P1 DML_CRX_PTX_N1 DML_CRX_PTX_P2 DML_CRX_PTX_N2 DML_CRX_PTX_P3 DML_CRX_PTX_N3

DML_RXP[0] DML_RXN[0] DML_RXP[1] DML_RXN[1] DML_RXP[2] DML_RXN[2] DML_RXP[3] DML_RXN[3]

DML_TXP[0] DML_TXN[0] DML_TXP[1] DML_TXN[1] DML_TXP[2] DML_TXN[2] DML_TXP[3] DML_TXN[3]

B8 A8 C6 B6 B5 A5 D4 B4

DML_CTX_PRX_P0 DML_CTX_PRX_N0 DML_CTX_PRX_P1 DML_CTX_PRX_N1 DML_CTX_PRX_P2 DML_CTX_PRX_N2 DML_CTX_PRX_P3 DML_CTX_PRX_N3

SKL_H_BGA_BGA @

+VCC_IO RC4 1 2 24.9_0402_1% PEG_COMP G2 PEG_RCOMP

Layout Notes:
Trace width=12 mils ,Spacing=15mil
Max length= 400 mils.

Security Classification Compal Secret Data

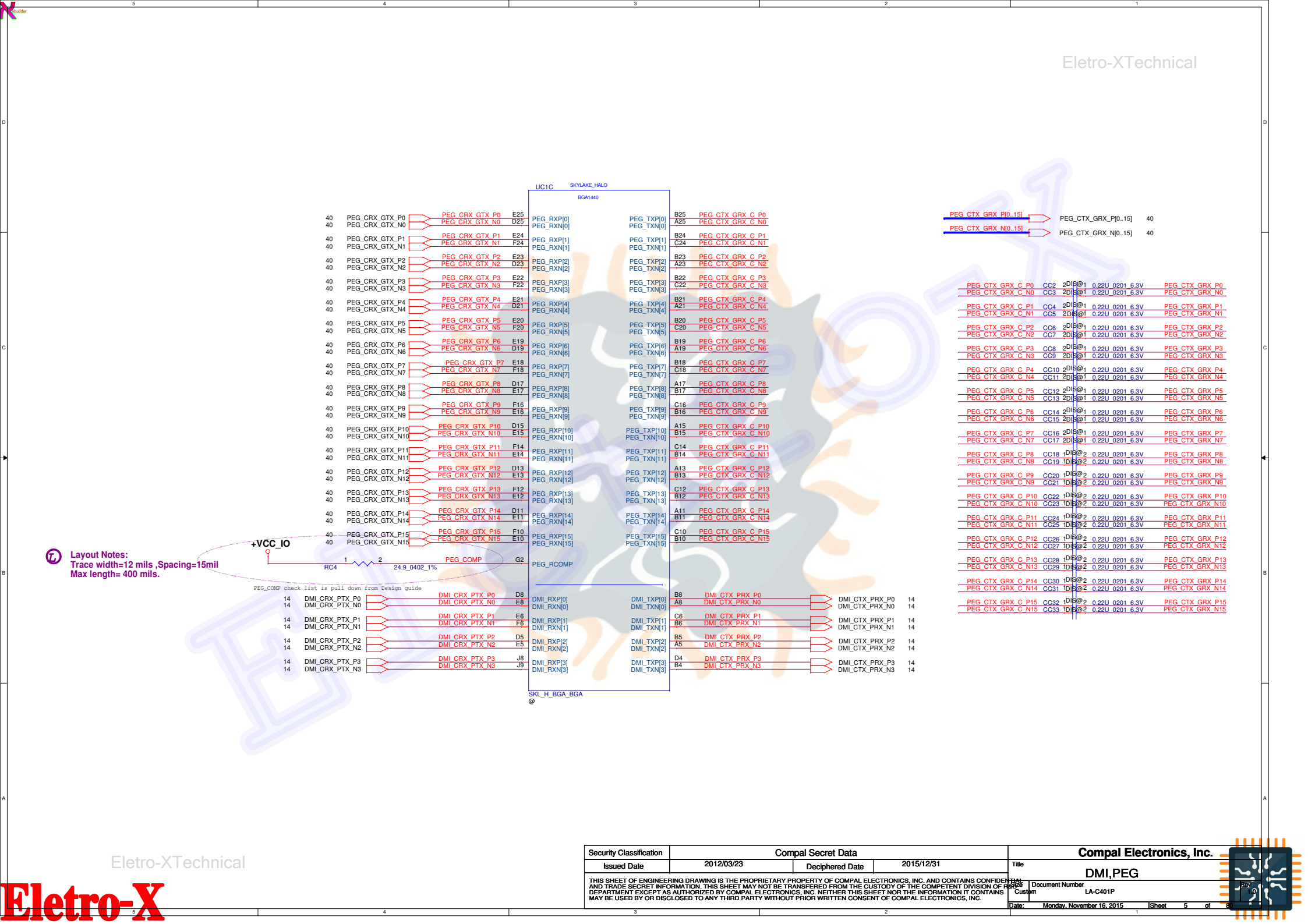
Issued Date 2012/03/23 Deciphered Date 2015/12/31

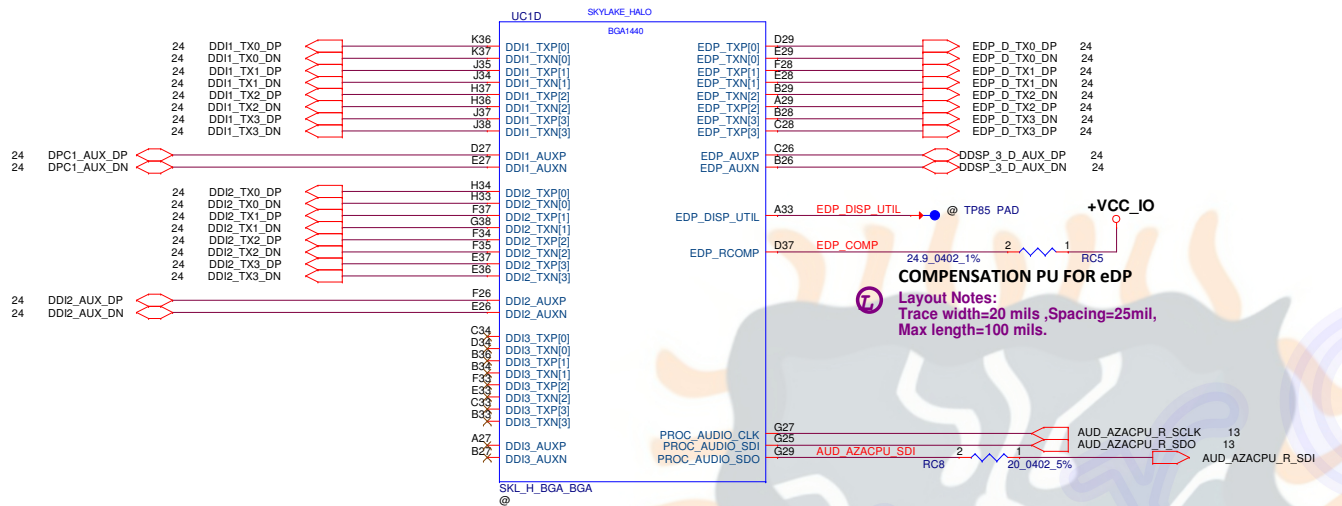
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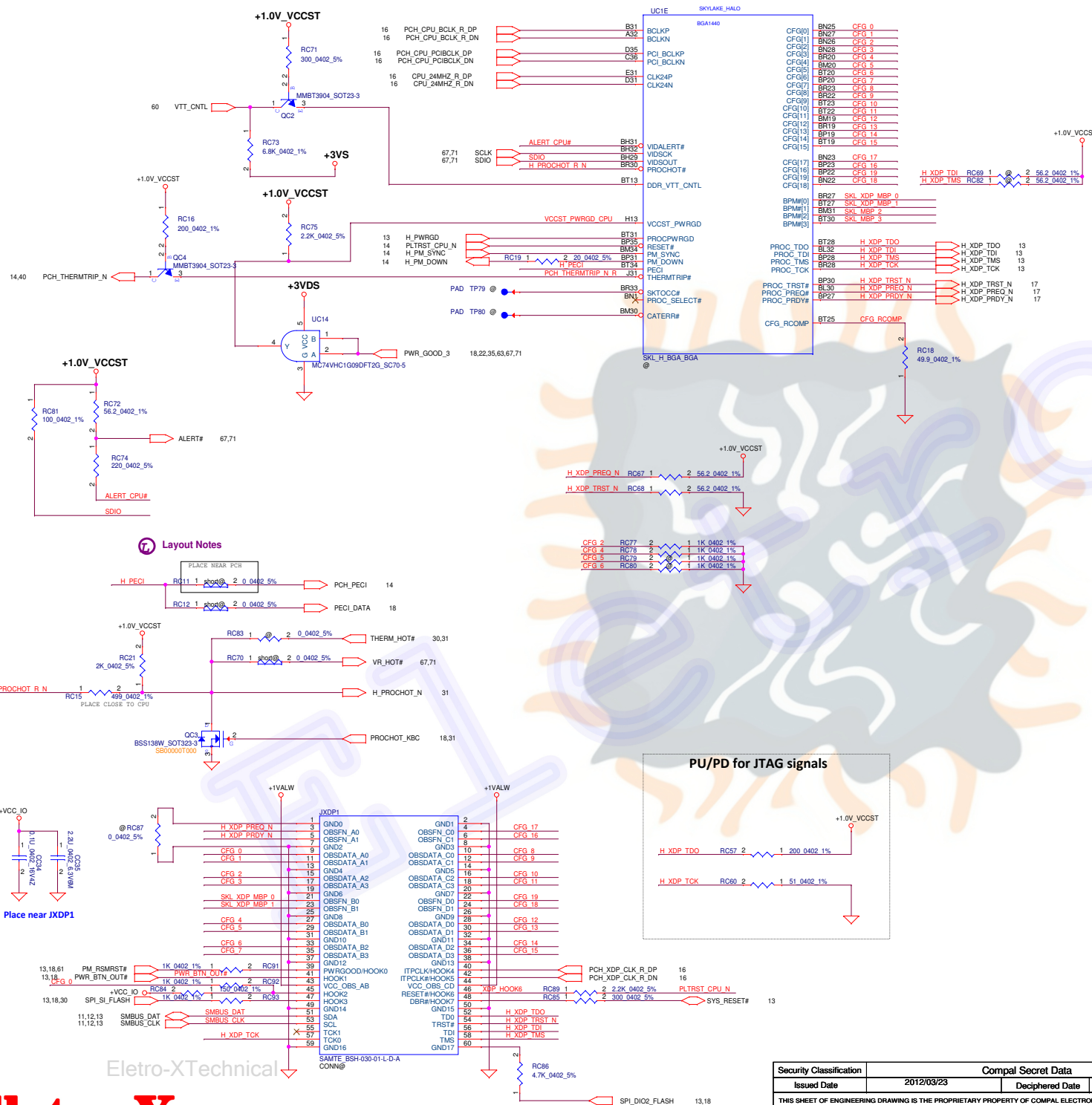
Compal Electronics, Inc.
DMI, PEG

Title Document Number LA-C401P

Date: Monday, November 16, 2015 Sheet 5 of 6

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Add 1k PD (open) resistor on the below CFG:

- 1).CFG[2]:Lanes number reserved.
- 2).CFG[4]:eDP enable.
- 3).CFG[5]: and [6]
- 4).CFG[7]

Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.

Intel recommends placing test points on the board for CFG pins.

.CFG[0]:Stall reset sequence after PCU PLL lock until de-asserted:

- 1=(Default) Normal Operation; No stall.
- 0=Stall.

.CFG[1]:Reserved configuration lane.
.CFG[2]:PCI Express*Static x16 Lane Numbering Reversal.

- 1=Normal operation
- 0=Lane numbers reversed.

.CFG[3]:Reserved configuration lane.

.CFG[4]:eDP enable:

- 1=Disabled.
- 0=Enabled.

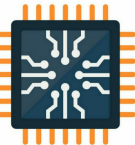
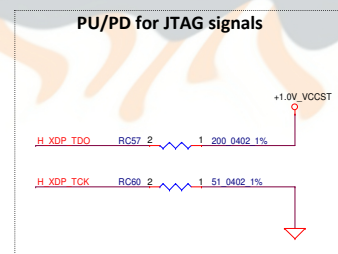
.CFG[6:5]:PCI Express* Bifurcation

- 00=1x8,2x4 PCI Express*
- 01=reserved
- 10=2x8 PCI Express*
- 11=1x16 PCI Express*

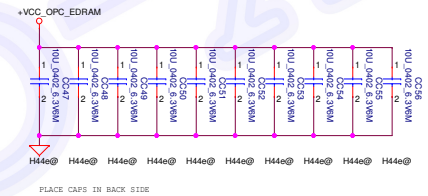
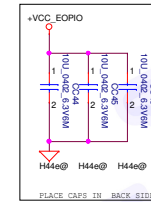
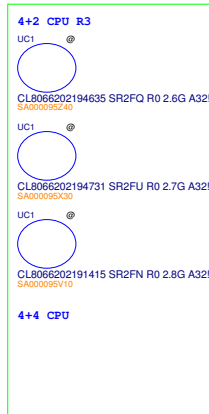
.CFG[7]:PEG Training:

- 1=(default) PEG Train immediately following RESET# de assertion.
- 0=PEG Wait for BIOS for assertion.

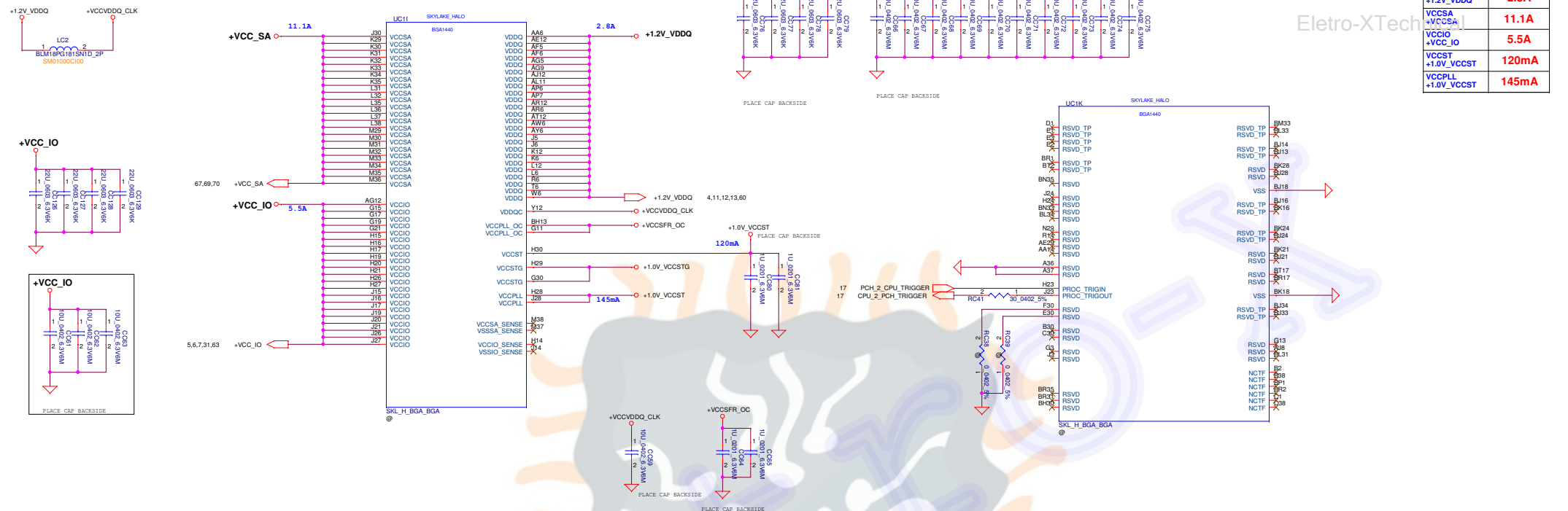
.CFG[19:8]:Reserved configuration lanes.



+VCC_OPC_EDRAM	2.6A
VCC_OPC_1F8 +1.8V_ALW	50mA



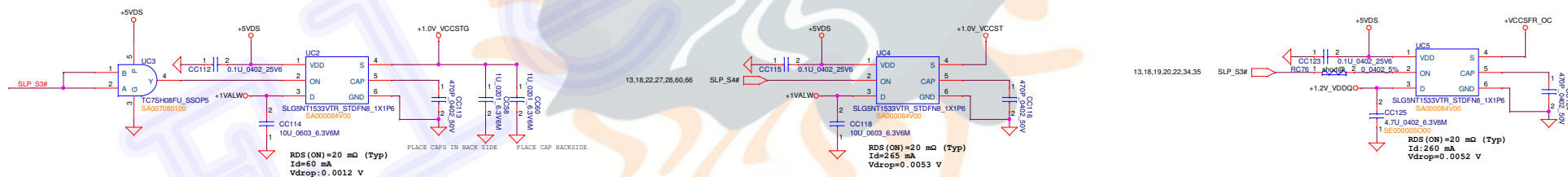
Power Name	Consumption
VDDQ	2.8A
+1.2V_VDDQ	11.1A
VCCSA	5.5A
VCCIO	120mA
+1.0V_VCCST	145mA



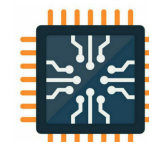
+1.0V_VCCSTG GENERATION

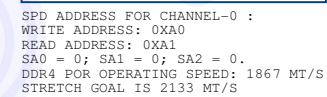
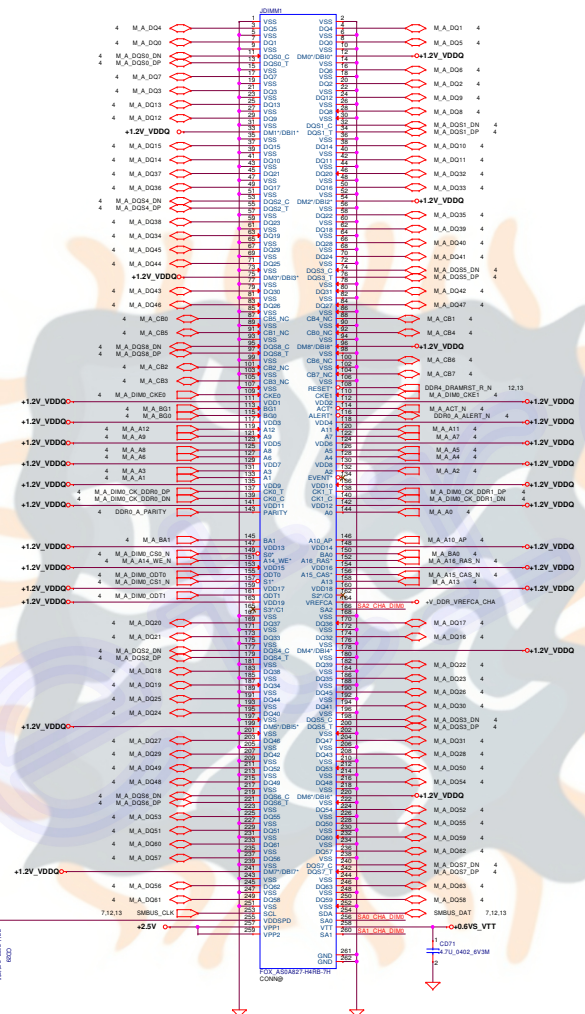
+1.0V_VCCST GENERATION

+VCCSFR_OC GENERATION

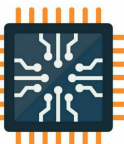


Security Classification				Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2012/03/23		Deciphered Date		2015/12/31	
Title		PWR,RSVD		Document Number		LA-C401P	
Revision		1.0		Date		Monday, November 16, 2015	
Sheet		10		of		80	



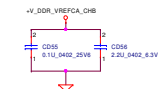


Eleto-X





PLACE THE CAP WITHIN 200 MILS
FROM THE SODIMM - 1



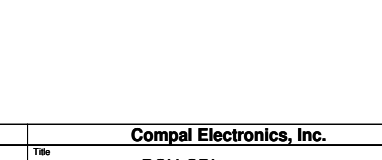
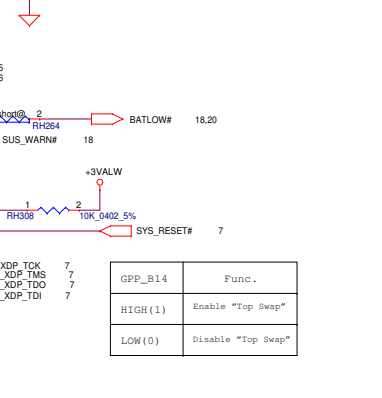
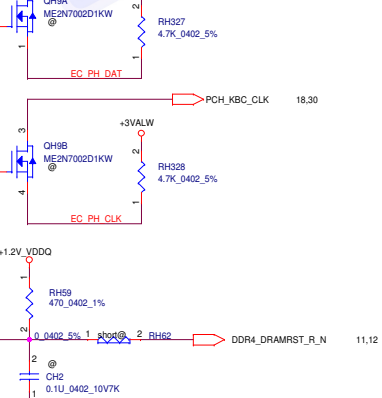
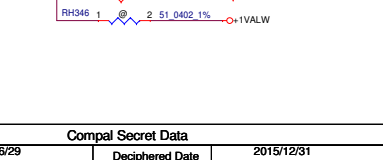
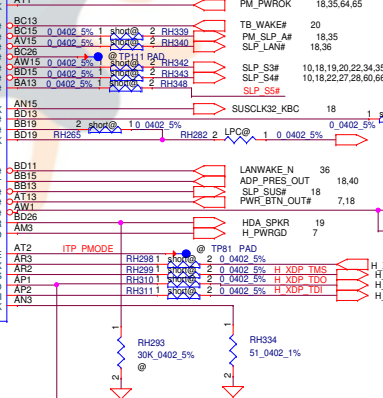
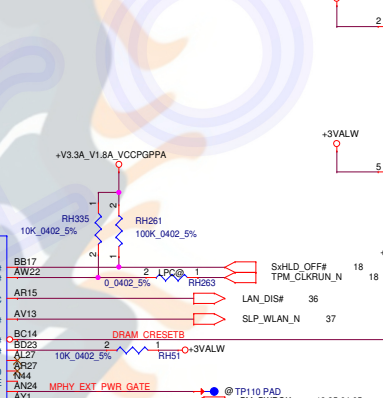
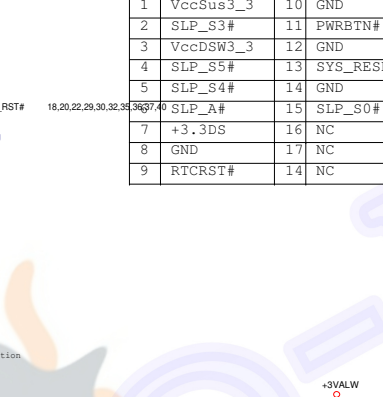
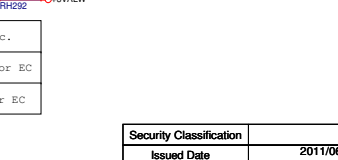
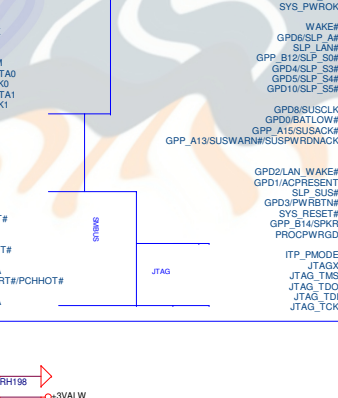
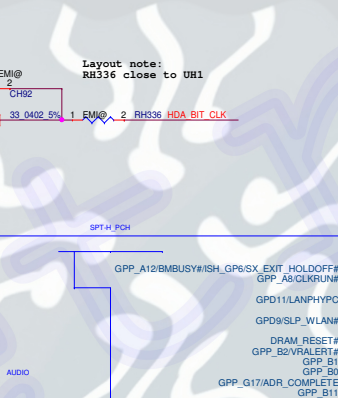
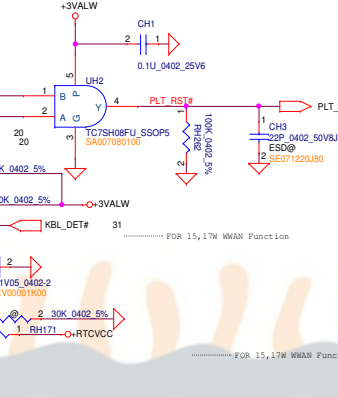
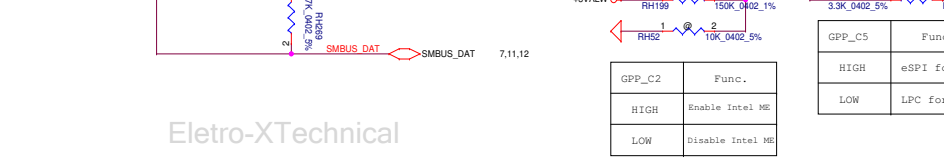
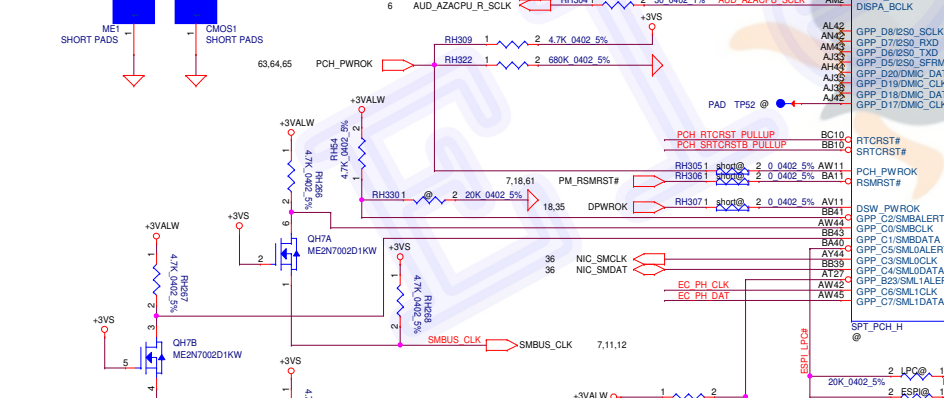
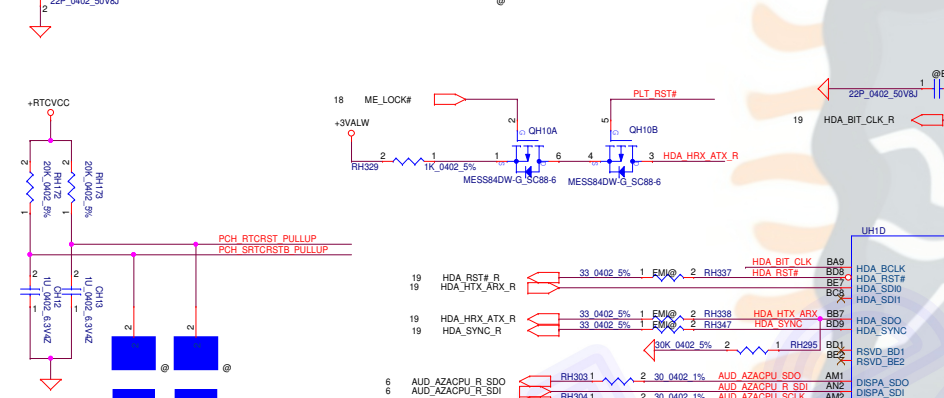
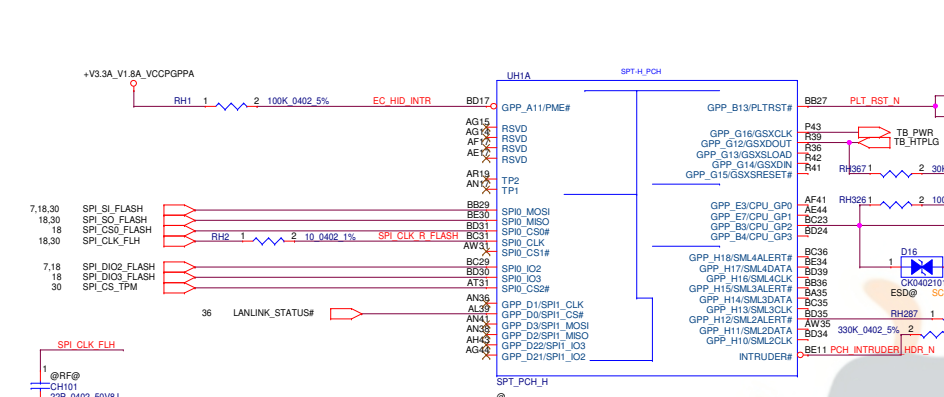
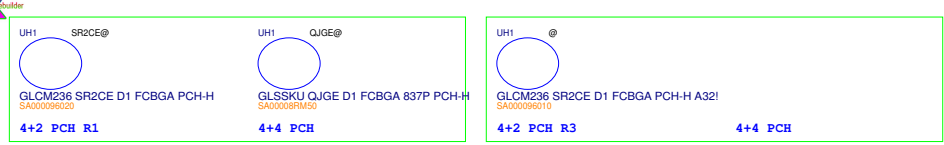
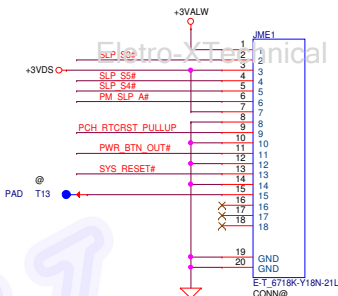
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Issued Date	2012/03/23	Deciphered Date	2015/12/31	
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Rev	0	Document Number	LA-C401P	
Rev	0	Model	Model	12
Rev	0	Pin	Pin	80



ME Debug Port

Pinout on customer's board,
as in the PDG, CDI #546884

Pin		Pin	
1	VccSus3_3	10	GND
2	SLP_S3#	11	PWRBTN#
3	VccDSW3_3	12	GND
4	SLP_S5#	13	SYS_RESET#
5	SLP_S4#	14	GND
6	SLP_A#	15	SLP_S0#
7	+3.3DS	16	NC
8	GND	17	NC
9	RTRCST#	18	NC



Eletro-XTechnical

Eletro-X

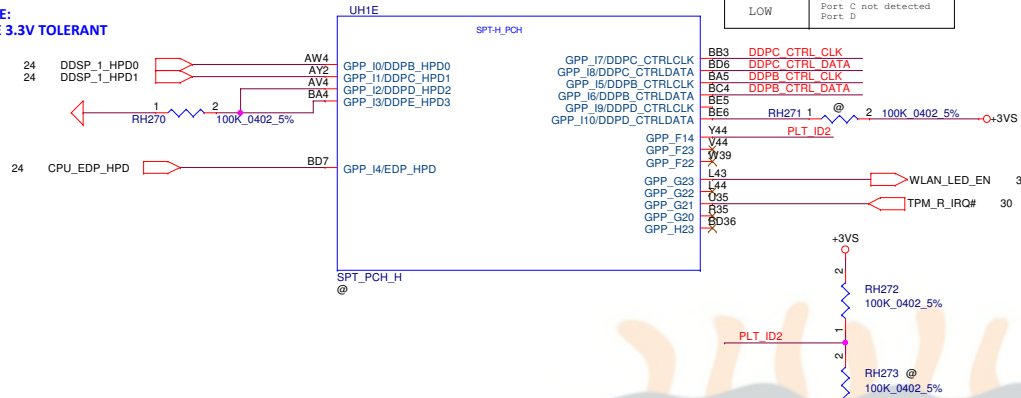
Security Classification	Compal Secret Data	Issued Date	2011/06/29	Deciphered Date	2015/12/31	Title	PCH-SPI
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						Date	Monday, November 16, 2015
						Sheet	13 of 80



HPD0 TO DP PORT0

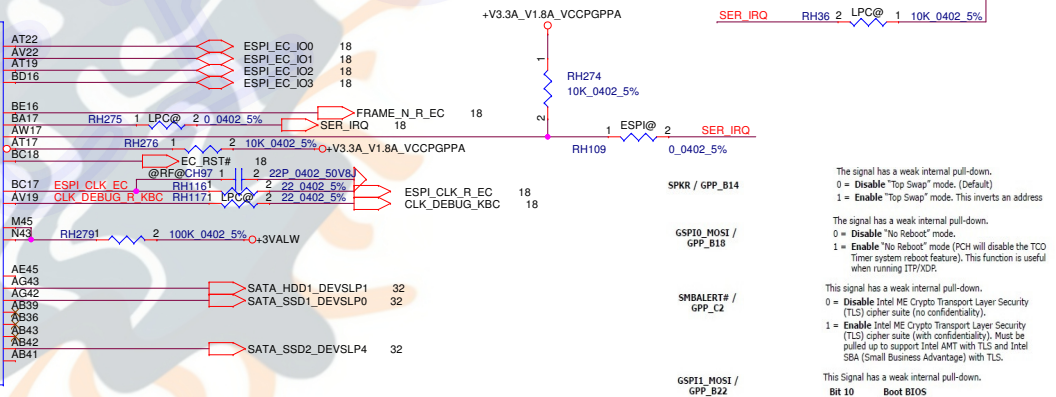
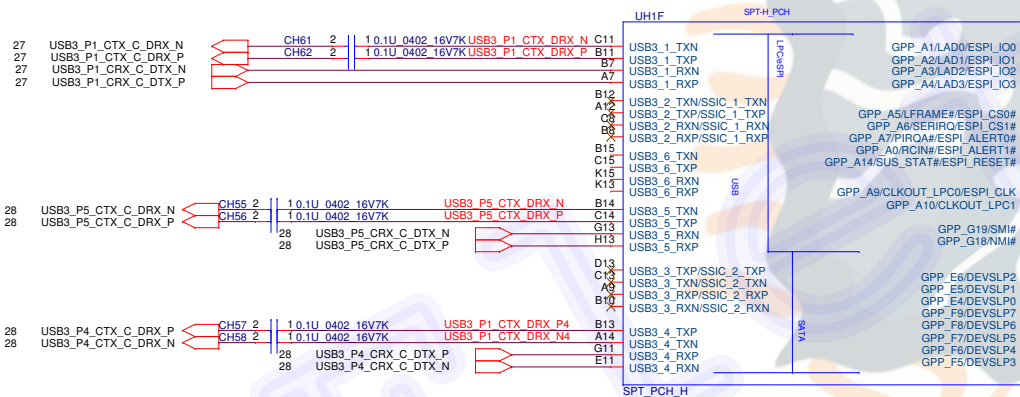
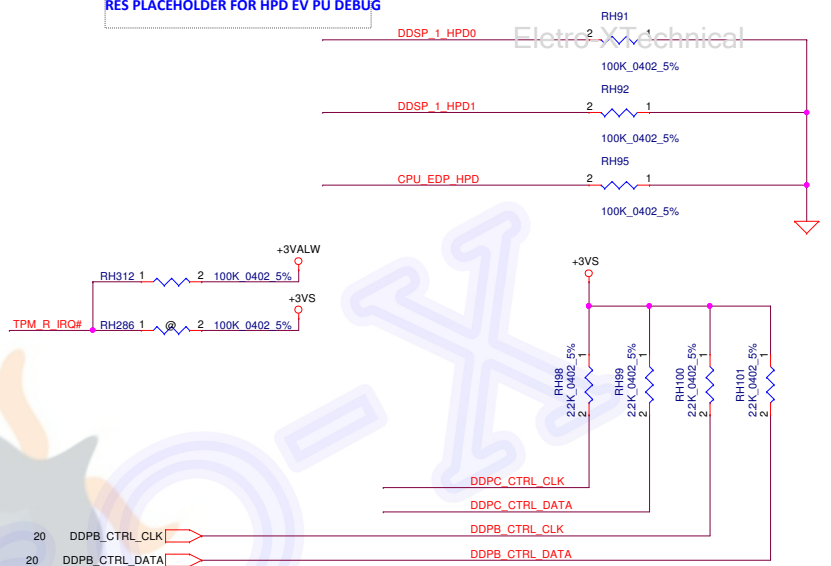
EDP HPD TO EDP

DESIGN NOTE:
HPD[2:0] ARE 3.3V TOLERANT



GPP_I6 GPP_I8 GPP_I10	Func.
HIGH	Port B Port C detected Port D
LOW	Port B Port C not detected Port D

DESIGN NOTE:
RES PLACEHOLDER FOR HPD EV PU DEBUG



Align DEVSLP pin assignment 1 host pin to 1 device pin as follows:

- SATA DEVSLP0 to DEVSLP Port0
- SATA DEVSLP1 to DEVSLP Port1
- SATA DEVSLP2 to DEVSLP Port2
- SATA DEVSLP3 to DEVSLP Port3
- SATA DEVSLP4 to DEVSLP Port4
- SATA DEVSLP5 to DEVSLP Port5

The signal has a weak internal pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode. This inverts an address

The signal has a weak internal pull-down.
0 = Disable "No Reboot" mode.
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDR.

This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

This signal has a weak internal pull-down.
Bit 10 Boot BIOS Destination
0 SPI
1 LPC

This signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (optional). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

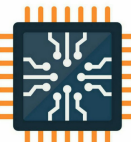
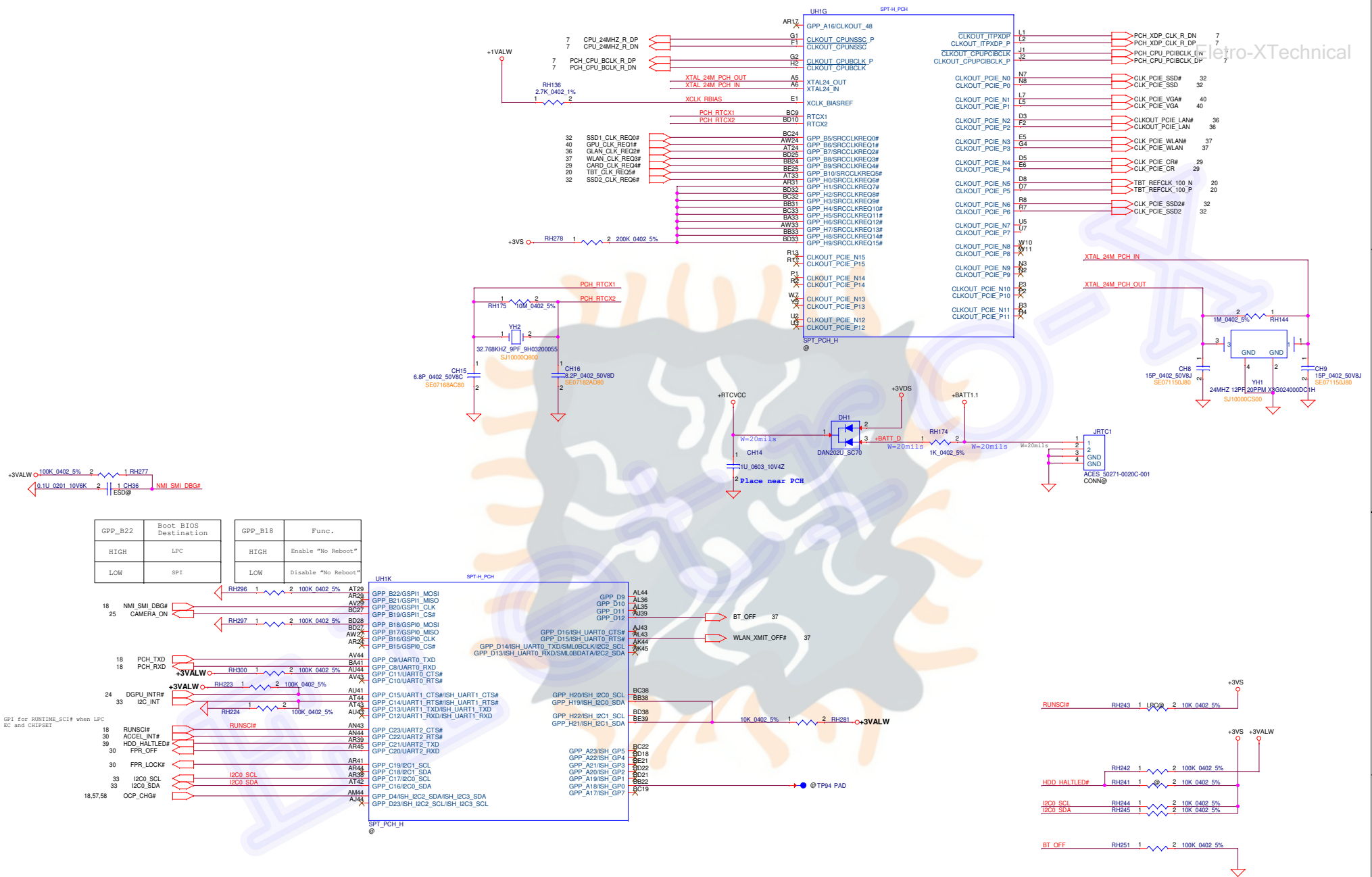
This signal has a weak internal pull-down.
0 = Port B is not detected.
1 = Port B is detected.

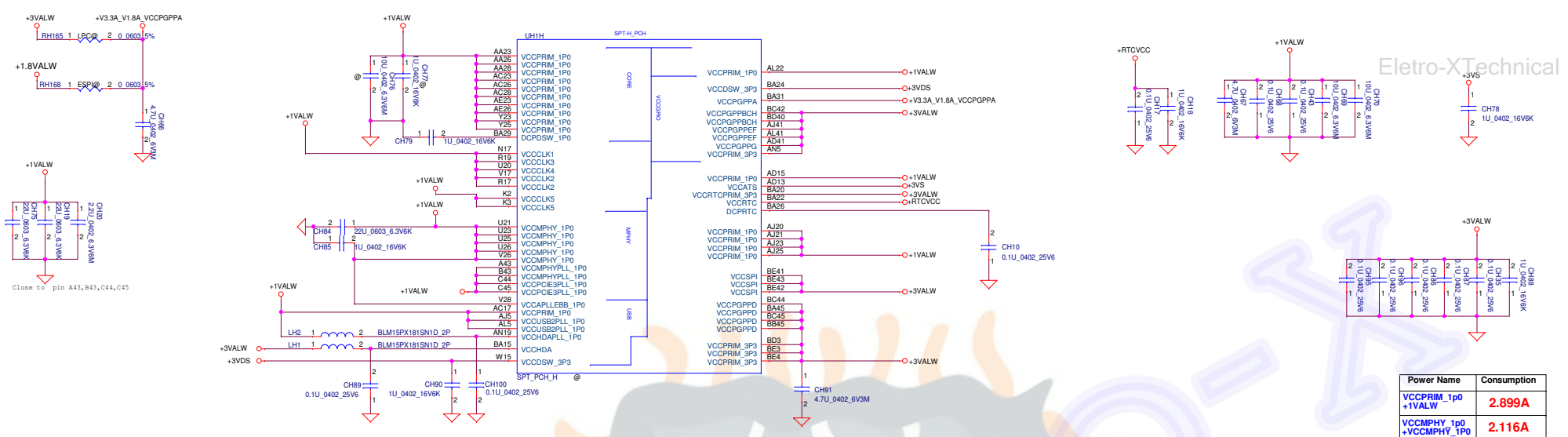
This signal has a weak internal pull-down.
0 = Port C is not detected.
1 = Port C is detected.

This signal has a weak internal pull-down.
0 = Port D is not detected.
1 = Port D is detected.

Eletro-XTechnical

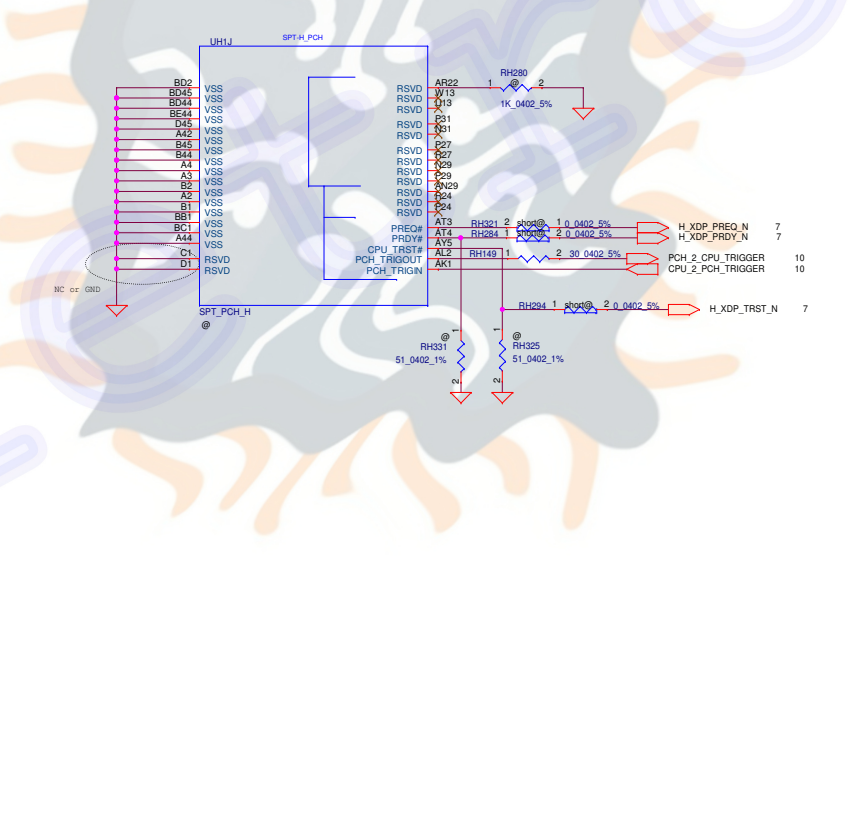
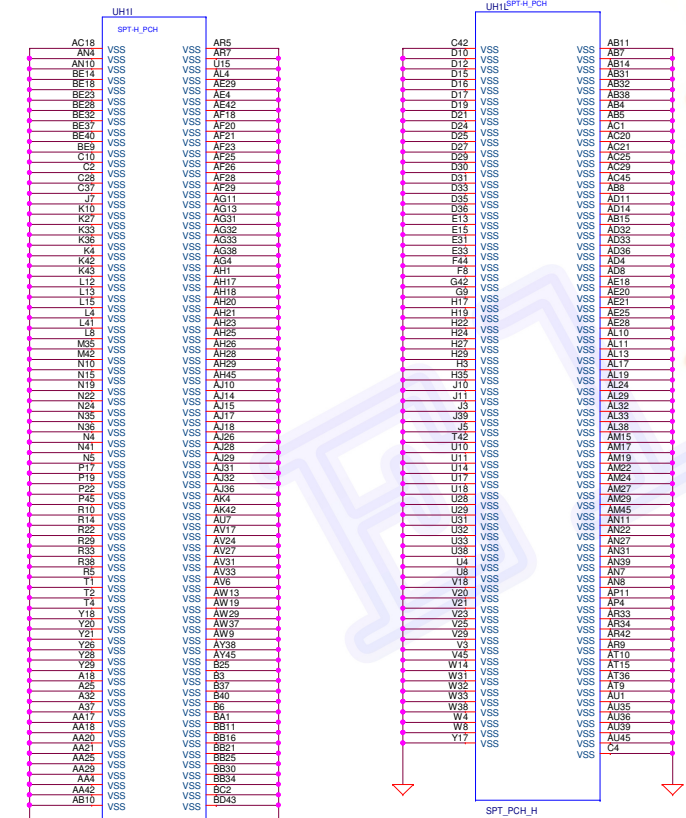
Eletro-X



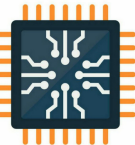


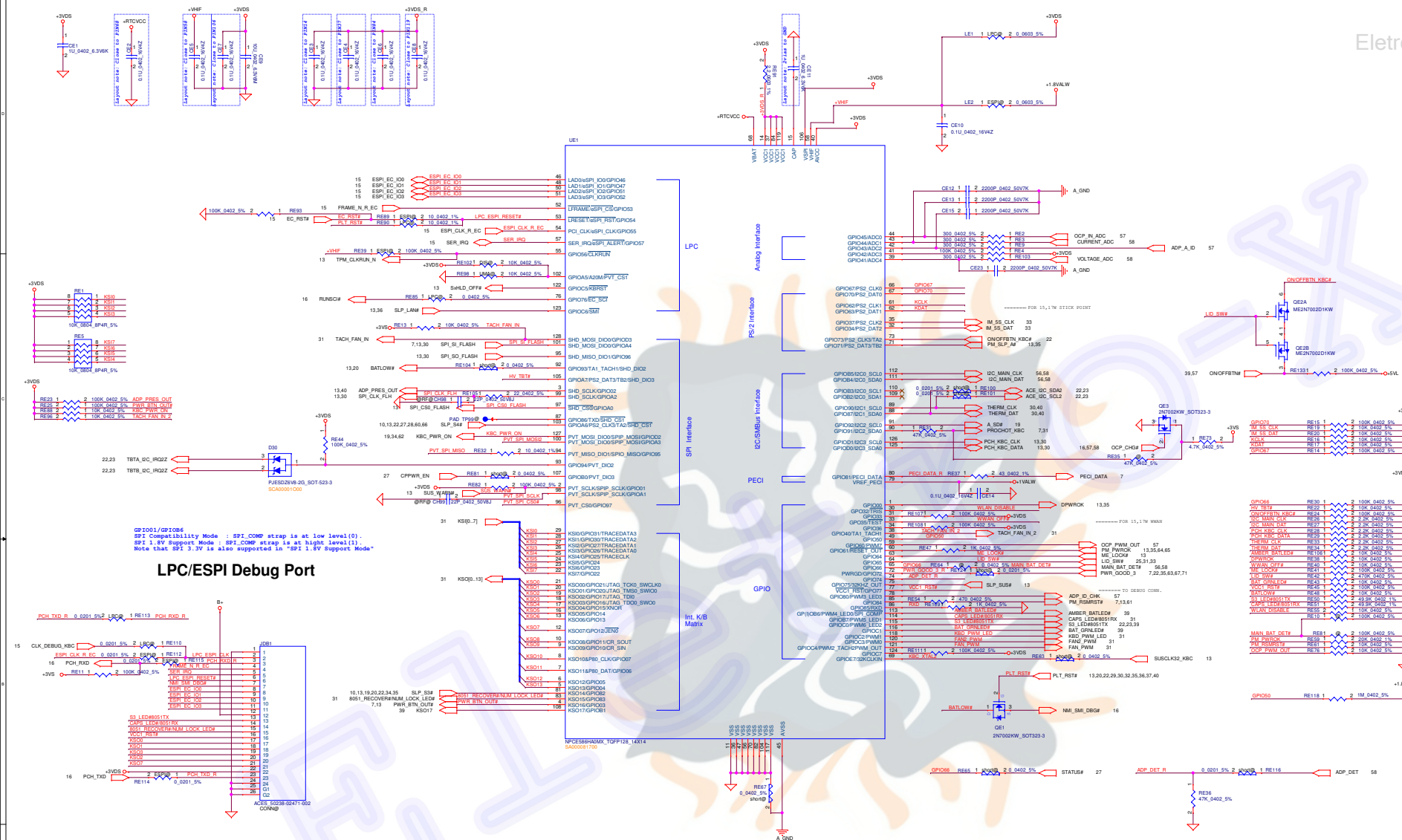
Eletro-XTechnical

Power Name	Consumption
VCCPRIM_1p0 +1VALW	2.899A
VCCMPHY_1p0 +VCCMPHY_1P0	2.116A

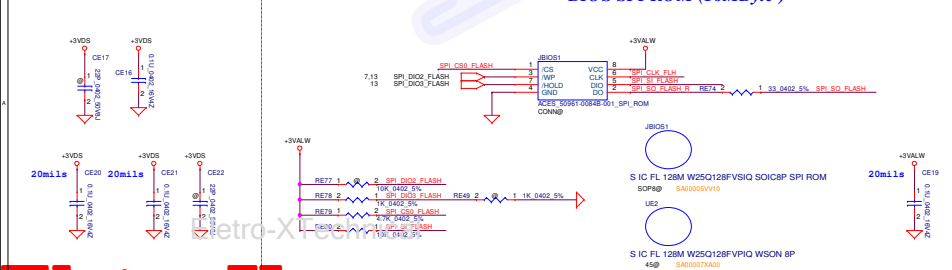


Voltage Rail	Voltage (V)	S0 Iccmax Current ¹ (A)
VCCPRIM_1p0	1.0	2.899
VCCCLK1	1.0	0.021
VCCCLK2	1.0	0.137
VCCCLK3	1.0	0.050
VCCCLK4	1.0	0.024
VCCCLK5	1.0	0.006
VCCMPHY_1p0	1.0	See Table 10-5
VCCDAPLL_1p0	1.0	0.033
VCCAPLLEBB_1p0	1.0	0.030
VCCPCIE3PLL_1p0	1.0	0.030
VCCUSB2PLL_1p0	1.0	0.012
VCCPGPPA	3.3	0.082
VCCPGPBCH	3.3	0.229
VCCPGPPD	3.3	0.078
VCCPGPPEF	3.3	0.036
VCCPGPPG	3.3	0.114
VCCPRIM_3p3	3.3	0.058
VCCDSW_3p3	3.3	0.065
VCCRTCPRIM_3p3	3.3	0.031
VCCRTC	3.3	0.029
VCCCLK1	1.8	0.014
VCCCLK2	1.8	0.007
VCCCLK3	1.8	0.060
VCCCLK4	1.8	0.036
VCCCLK5	1.8	0.030
VCCMPHY_1p0	3.3	0.117
VCCDSW_3p3	3.3	0.195
VCCRTCPRIM_3p3	3.3	<0.001
VCCRTC	3.0	<0.001

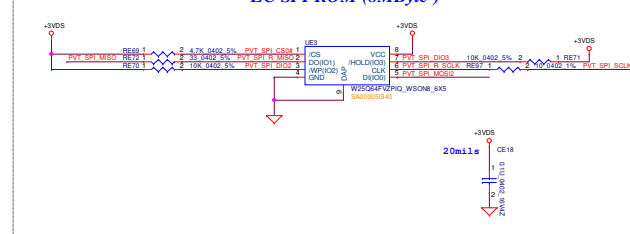





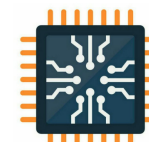
BIOS SPI ROM (16MByte)

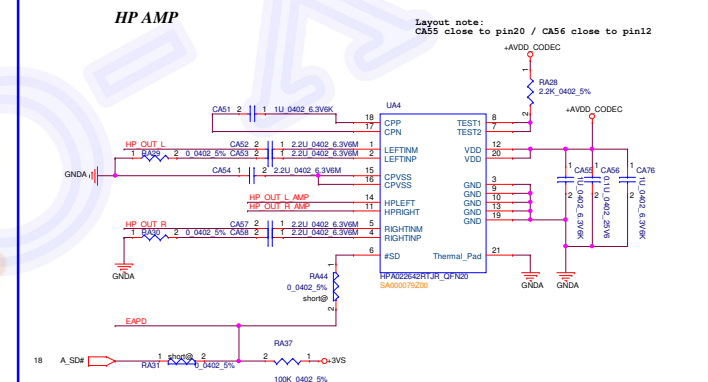
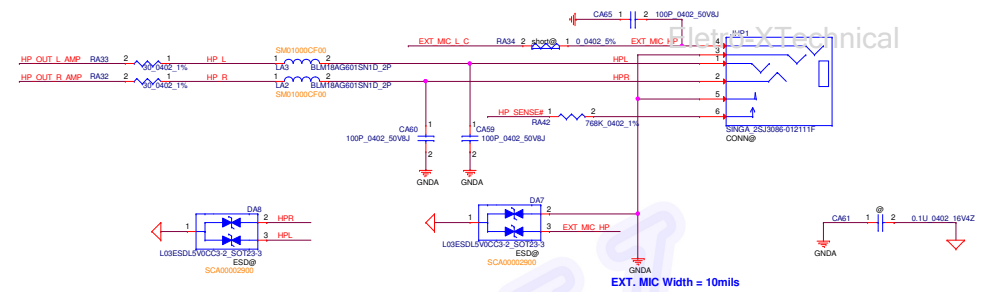


EC SPI ROM (8MByte)



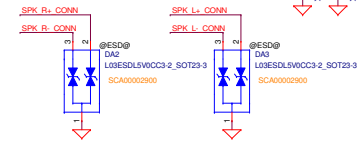
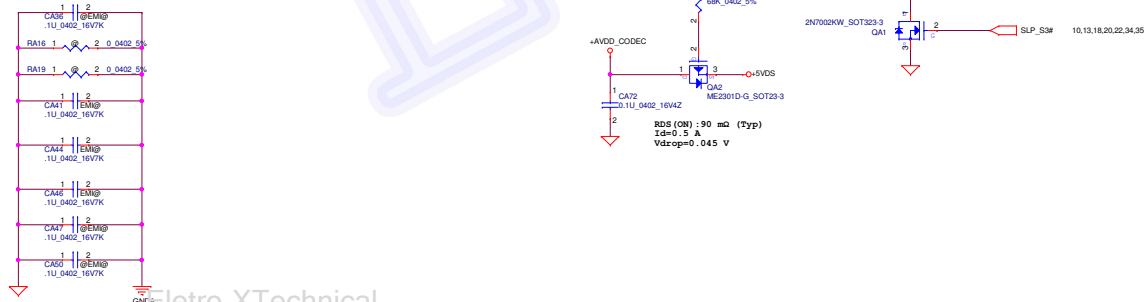
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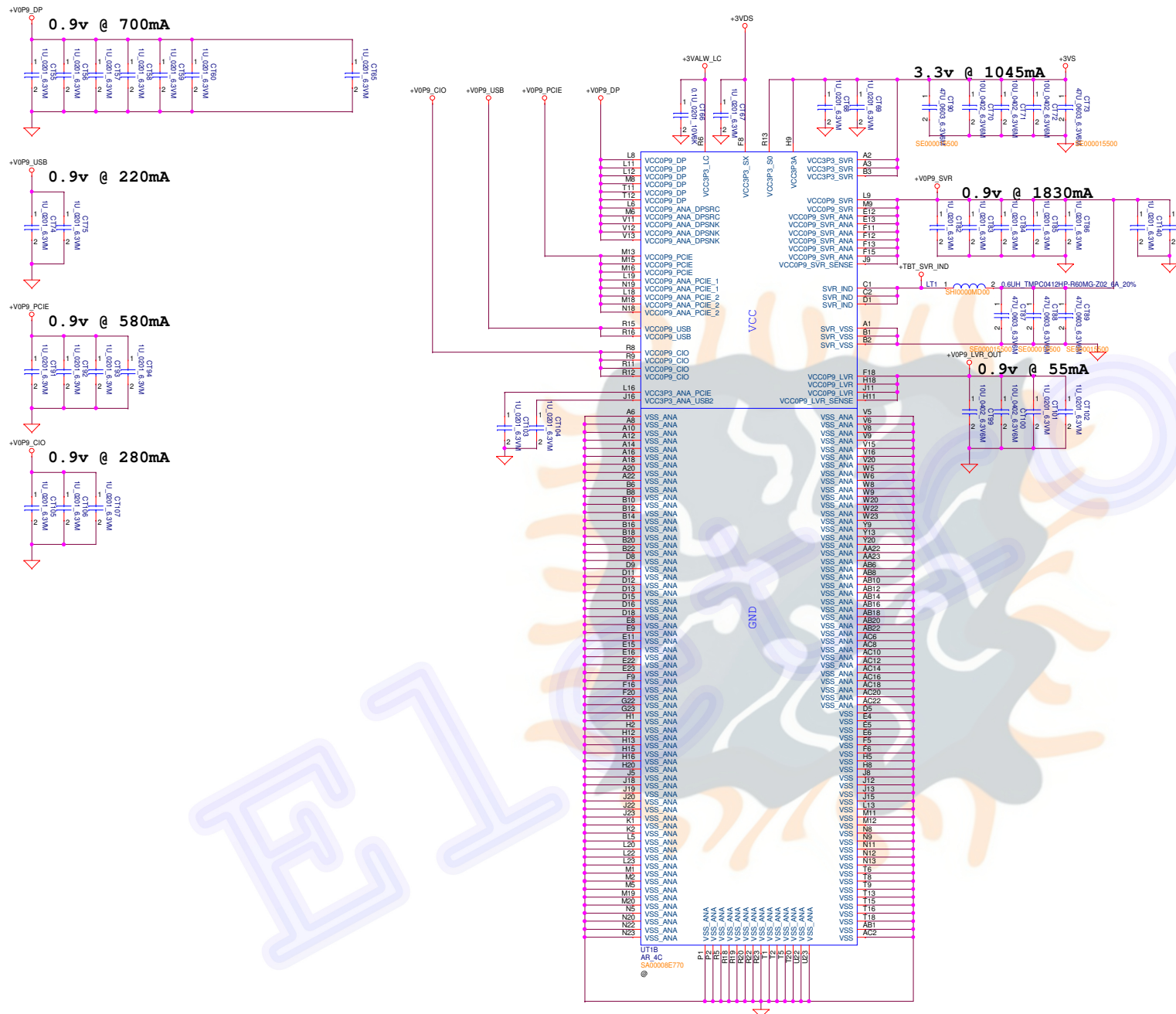
SPK conn

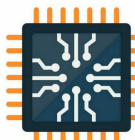
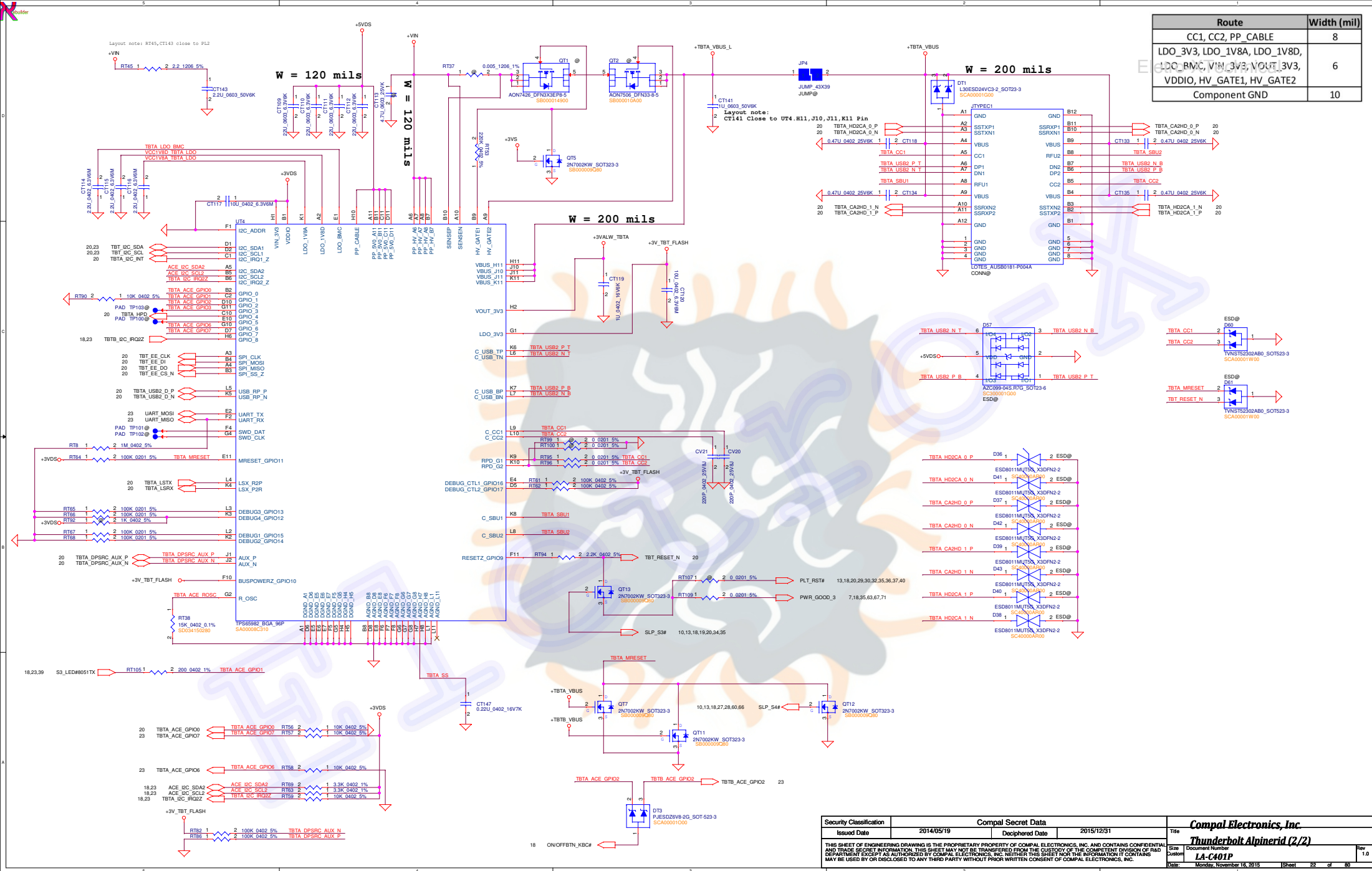
SPK signal width=40mil



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Route	Width (mil)
CC1, CC2, PP, CABLE	8
LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VIN_3V3, VOUT_3V3, VDDIO, HV_GATE1, HV_GATE2	6
Component GND	10

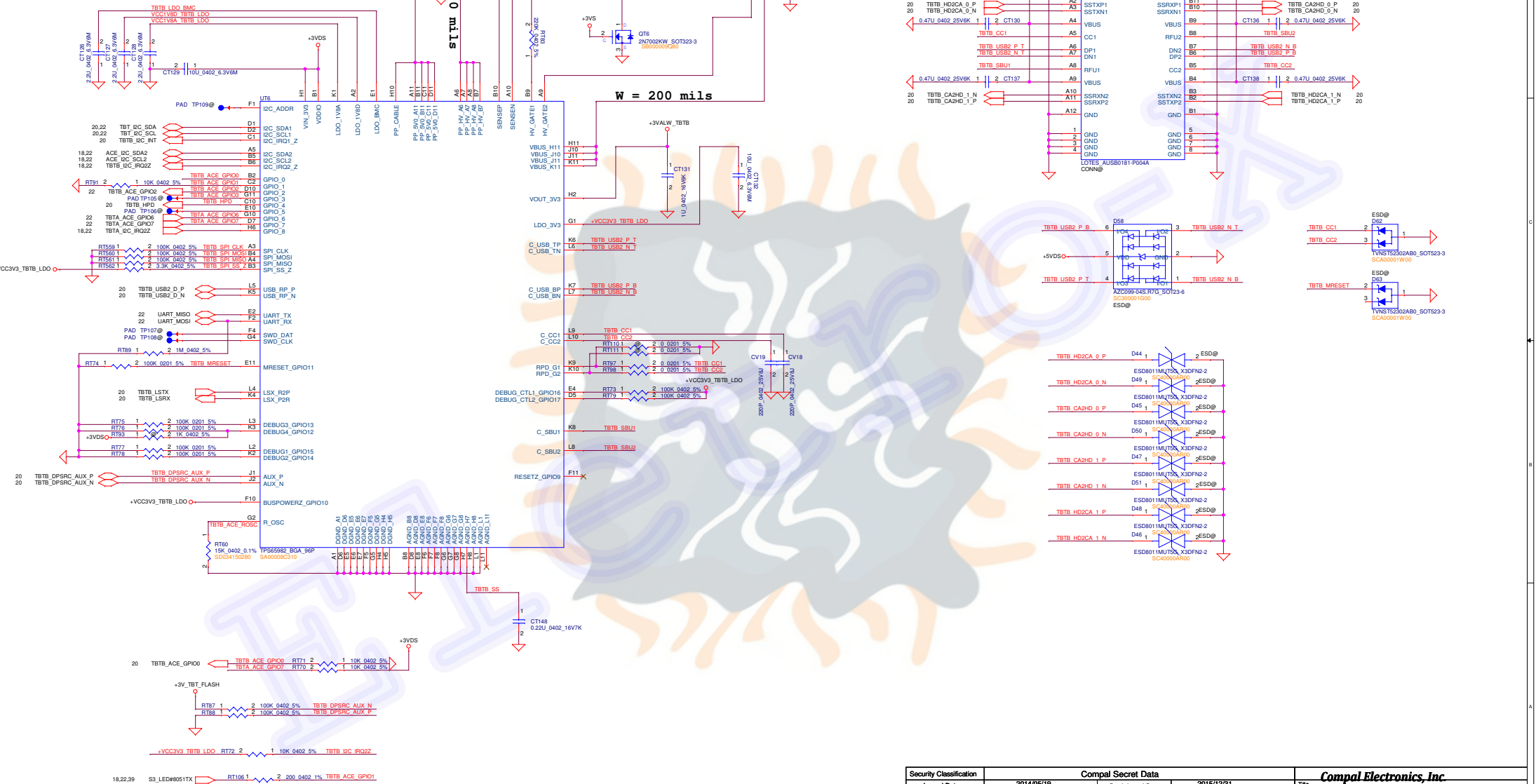
W = 120 mils

W = 120 mils

W = 200 mils

W = 200 mils

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Size	Document Number	Rev		
Custom	LA-CA01P	1.0		
Date	Monday, November 16, 2015	Sheet	23	of 80

Eletro-XTechnical

Eletro-X



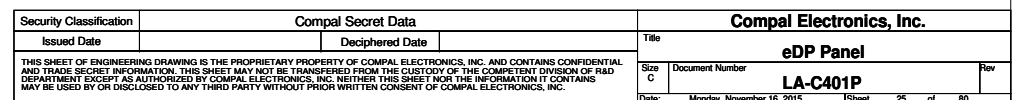


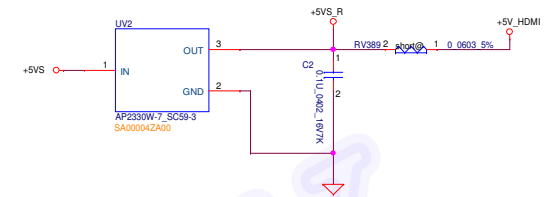
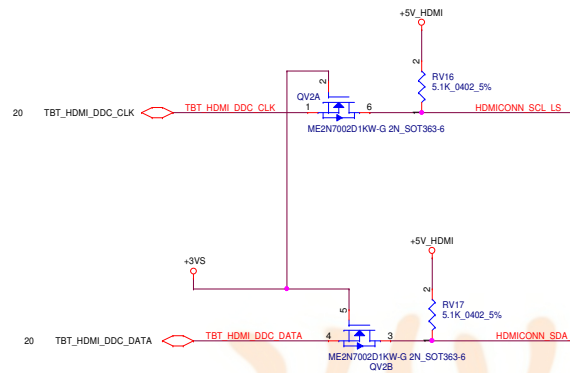
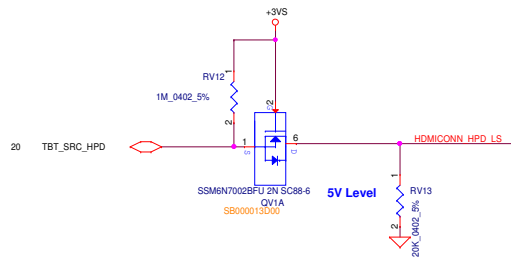
Eleto-XTechnical

To EDP Conn.

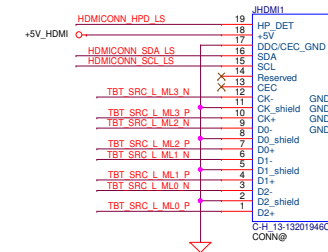
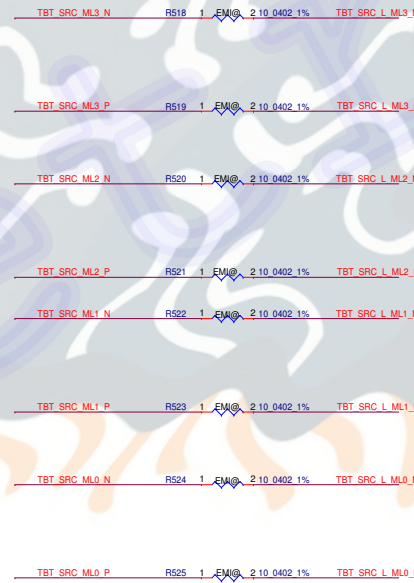
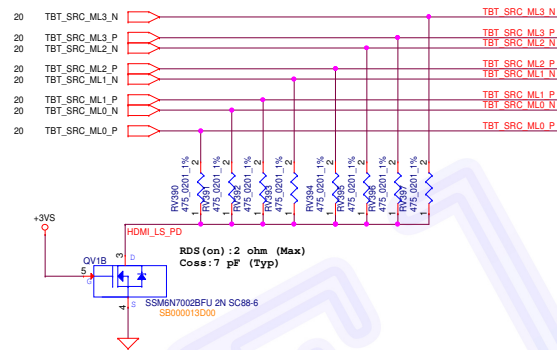
DGPU_SELECT#	UMA_ONLY#	Mode option
1	0	Invalid config
0	1	HP Hybrid SG
0	0	DGPU only
1	1	UMA/Headless SG

eDP PANEL Conn.



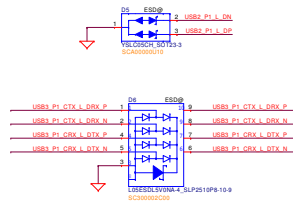
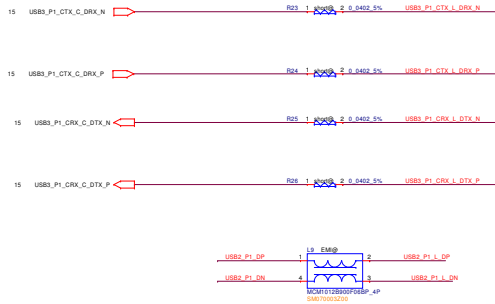


5V PULL UP IN CONNECTER SIDE

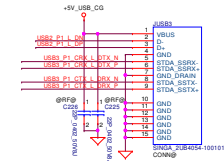


MB_USB 3.0 With charger function (Charging Port)

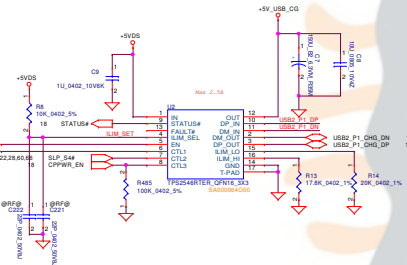
Eletro-XTechnical



USB3.0 / USB2.0 Port1 (Left Side)



USB charger



State	S0	S3, S4, S5
Mode	CDP	DCP
Control pin	CTL1 CTL2 CTL3 ILIM_SEL	CTL1 CTL2 CTL3 ILIM_SEL
	1 1 1 1	0 0 1 1

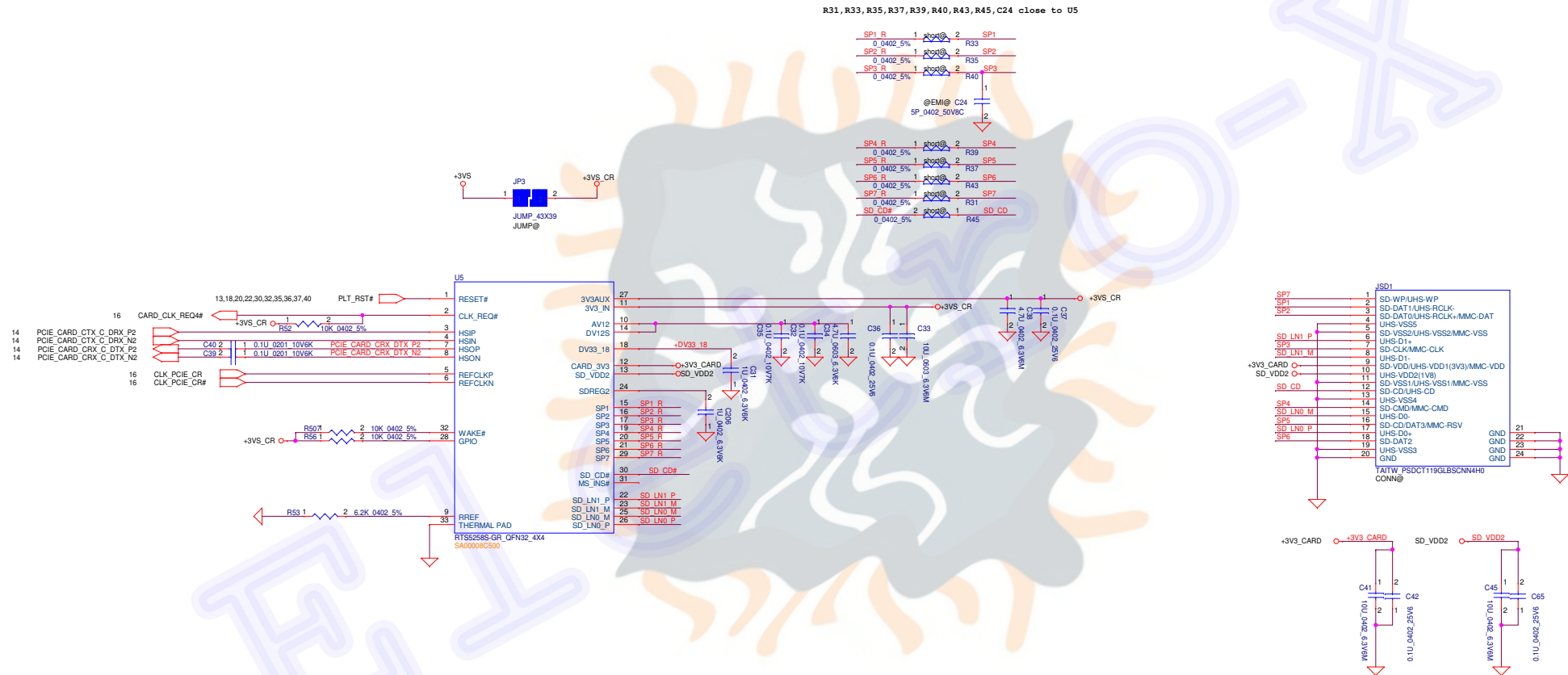
CDP:Charging Downstream Port
DCP:Dedicated Charging Port

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Issued Date	2014/05/19	Discontinued Date
2015/12/31		
Rev	1.0	1.0
Rev	1.0	1.0
Rev	1.0	1.0

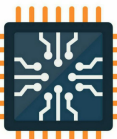
Eletro-XTechnical

Eletro-X

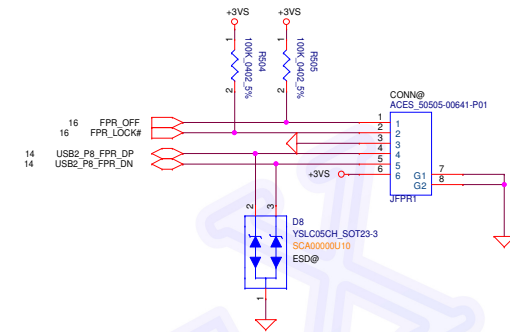




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				LA-C401P			1.0	
				Date	Monday, November 16, 2015		Sheet	29



Eletro-XTechnical



MMBT3904_SOT23-3
SB0000006A00

Q6

1 2 3

C49

2200P_0402_50V7K

1 2

0.1U_0402_50V4Z

1 2

3V3

R73

33K_0402_5%

1 2

3V3

1 2 3 4 5

18

VDD

D+

D-

T_CRIT#

SCL

SDA

ALERT#

GND

8

7

6

5

DC I2C CLK

DC I2C DAT

THERM_HOT#

7.31

PLACE CLOSE TO CPU

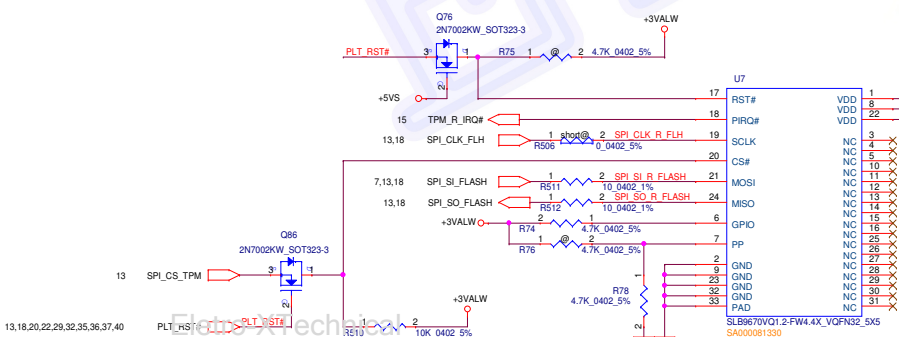
NC17718W_MS08P

S4000067P00

Address:1001_1001 (R)

Address:1001_1000 (W)

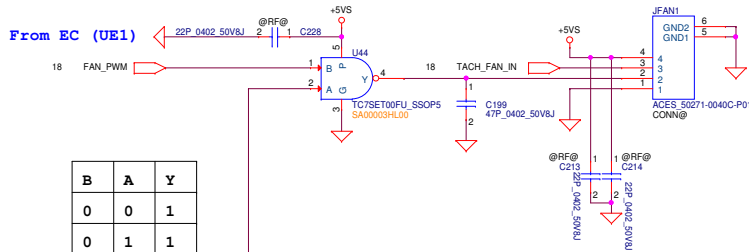
The schematic diagram shows a DC-DC converter circuit. A +3V5 input is connected to a voltage divider consisting of resistors R69 (10K_0402_5%) and R68 (10K_0402_5%). The output of the divider is connected to the gate of MOSFET O89A (2N7002KDW_SOT363-6). The MOSFET's source is connected to ground, and its drain is connected to the output of the converter. A diode O89B (2N7002KDW_SOT363-6) is connected in parallel with the MOSFET's drain. The output of the converter is connected to the THERM module pins 18,40, which are labeled DC_12C_CLK and DC_12C_DAT.



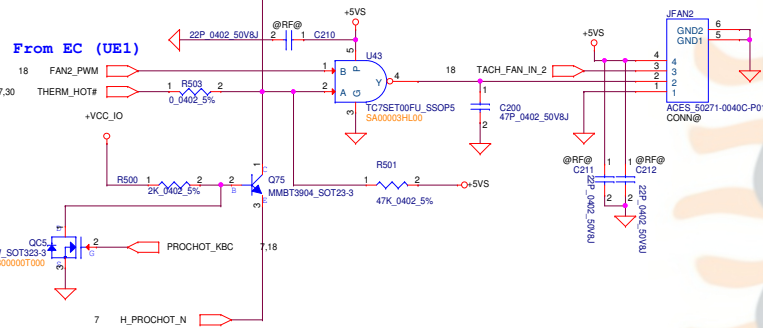
Security Classification	Compal Secret Data			Compal Electronics, Inc. G-sensor & TPM&Thermal & FP		
Issued Date	2014/05/19	Deciphered Date	2015/12/31	Title		
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					LA-C401P	1.0
				Date:	Monday, November 16, 2015	Sheet 30 of 80



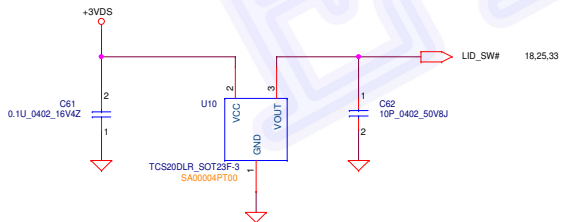
Fan Control Circuit



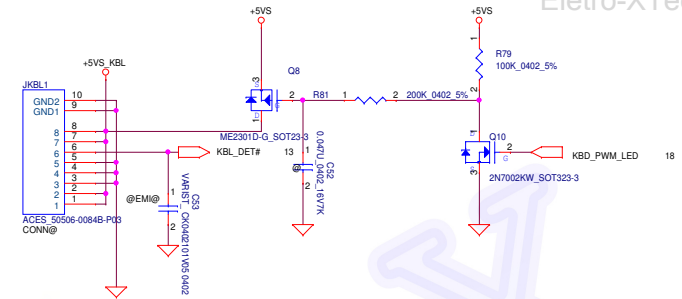
B	A	Y
0	0	1
0	1	1
1	0	1
1	1	0



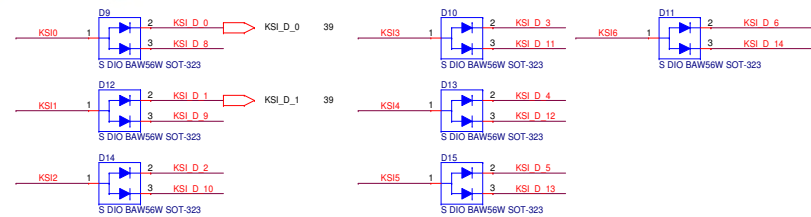
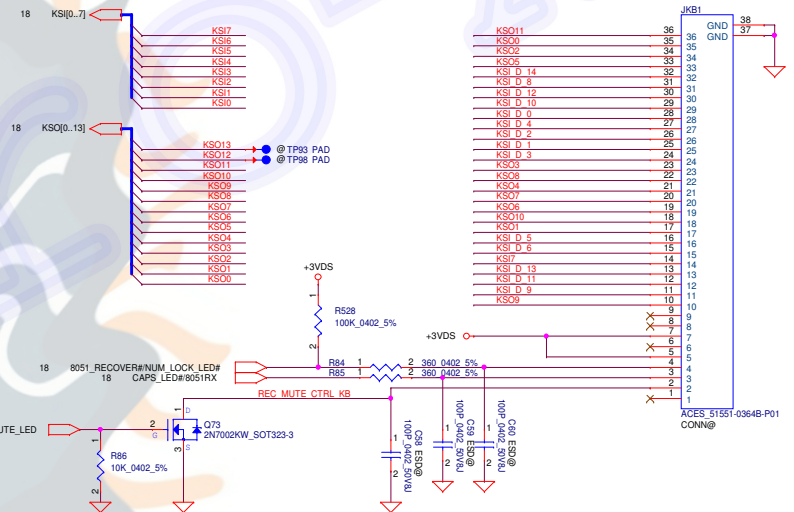
Lid Switch

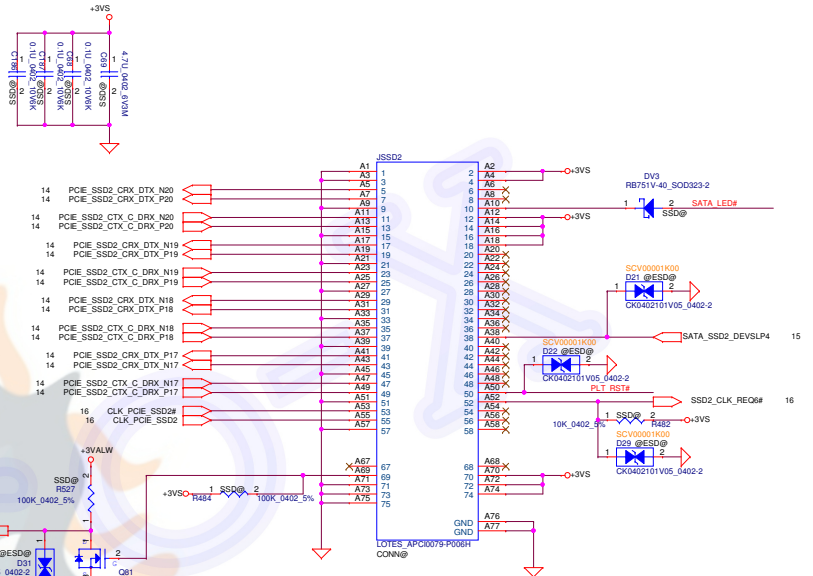


KB backlight Conn



Keyboard conn





2.5" SATA HDD

The diagram illustrates the internal circuitry of a 2.5-inch SATA HDD. It includes a power input section with a 10.0kV 1N4148 diode and a 0.1uF 50V capacitor. A microcontroller (U1) is connected to various pins, including SATA_HDD1_DEVSLP1, SATA_HDD1_CTX_DRX_P1B, SATA_HDD1_CTX_DRX_N1B, SATA_HDD1_CRX_C_DTX_N1B, and SATA_HDD1_CRX_C_DTX_P1B. A detailed pinout for the SATA connector is provided, showing connections for +5V, GND, and data lines (D0-D15).

Pinout Details:

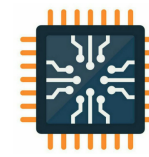
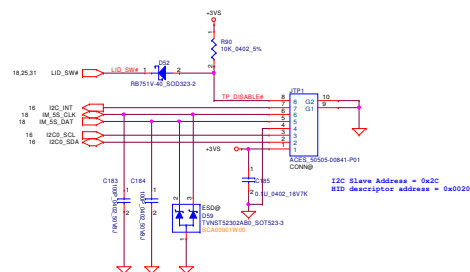
Pin	Signal	Component
1	+5V	U1
2	GND	U1
3	GND	U1
4	GND	U1
5	GND	U1
6	GND	U1
7	GND	U1
8	GND	U1
9	GND	U1
10	GND	U1
11	GND	U1
12	GND	U1

StarCap 111010-000000-G4-R

COMPAL

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Part No.	111010-000000-000000	Issued	95	01

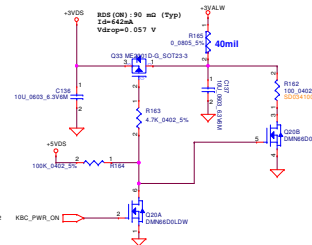
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Issued Date	2014/05/19	Deciphered Date	2015/12/31	Size	M2 SSD & 2.5" HDD	
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				Date	Monday, November 16, 2015	
				Sheet	32 of 80	



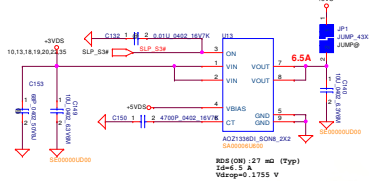
DC/DC

Eletro-XTechnical

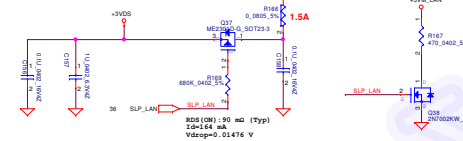
+3VDS TO +3VALW



+3VDS to +3VS Transfer

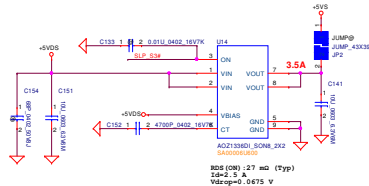


+3VDS to +3VM_LAN Transfer



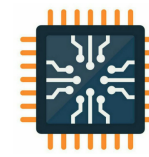
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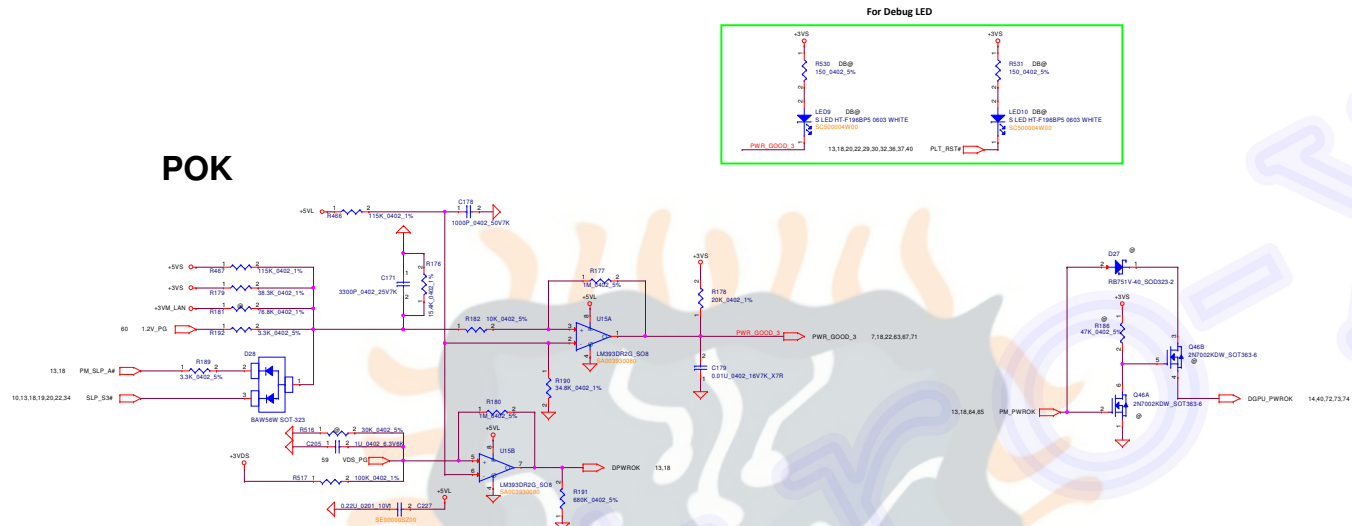


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Issued Date	2014/05/19	Discontinued Date	2015/12/31	Rev
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Eletro-XTechnical

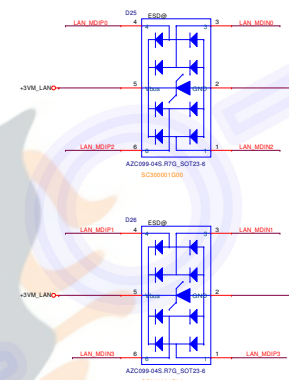
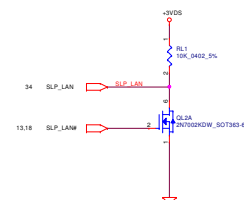
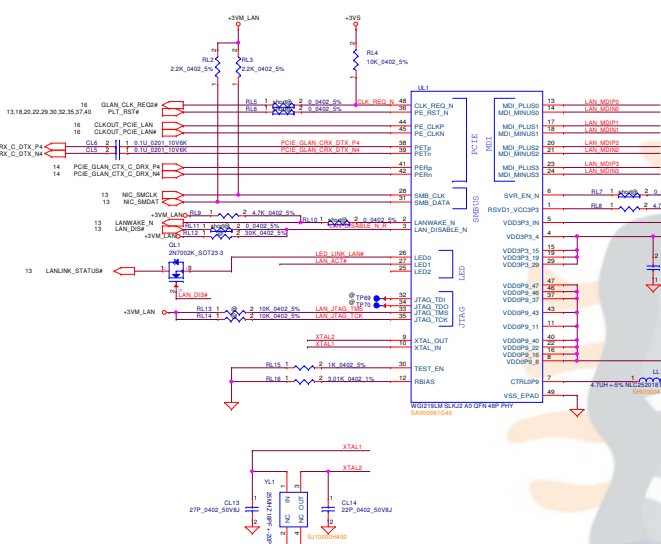
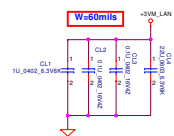


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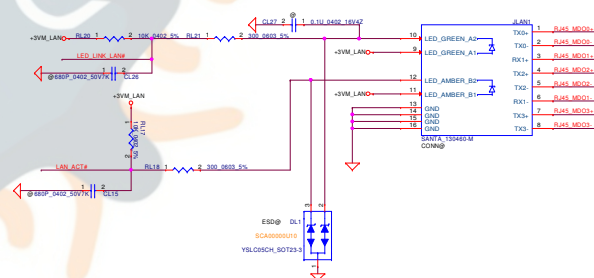


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Doc No	LA-C401P			Rev 1.0
Date	Monday, November 18, 2015	Time	10:48:01	Page 1 of 1

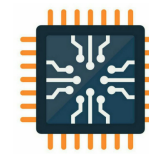




RJ-45 CONN.



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			Doc	LA-CA01P

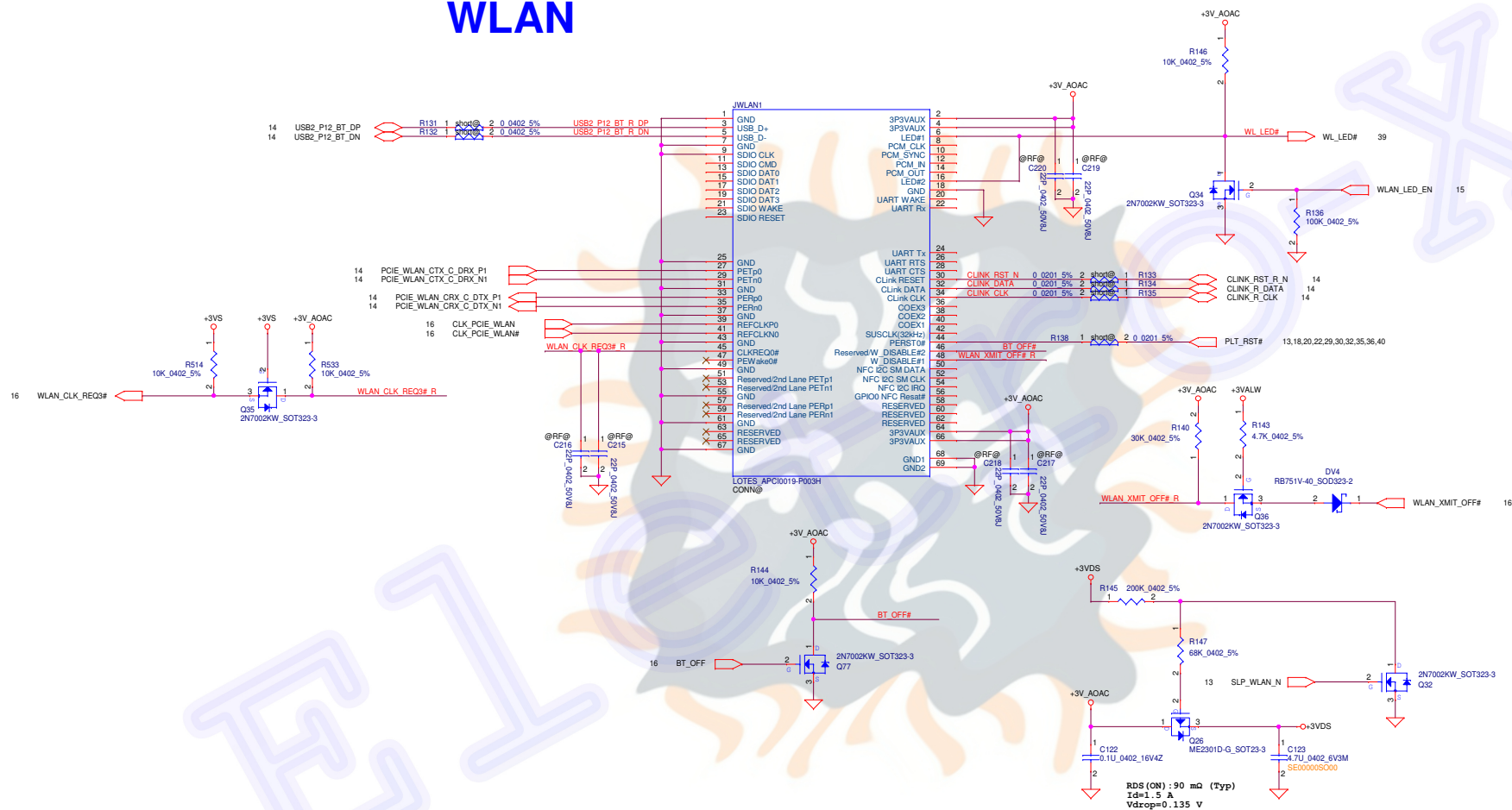


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Issued Date	2014/05/19	Deciphered Date	2015/12/31
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WLAN

Document Number	LA-C401P
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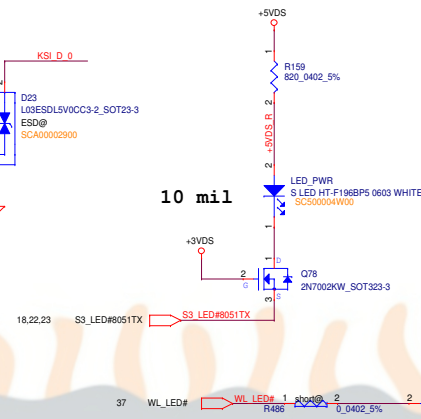
Size	Document Number	Rev
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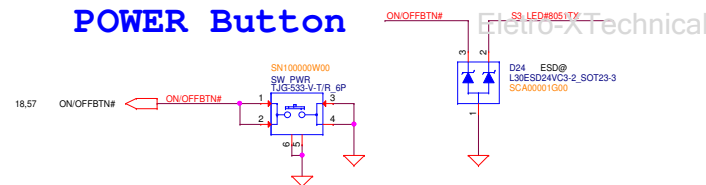
Wifi & mute Button



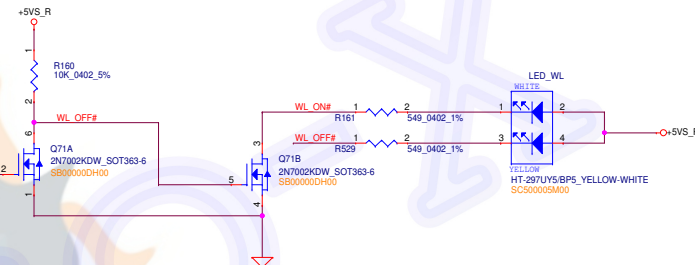
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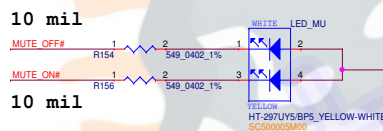
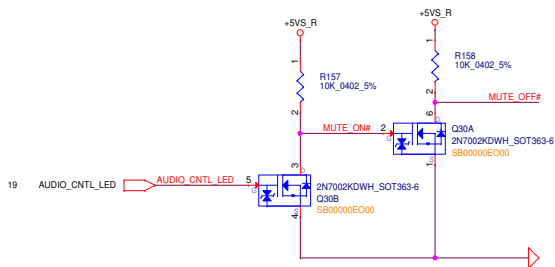
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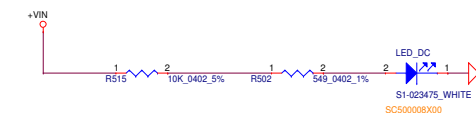
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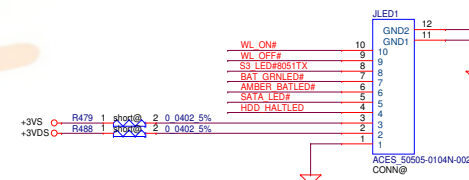
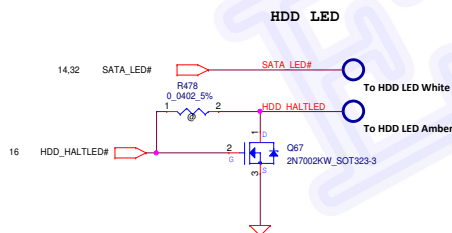
MUTE LED



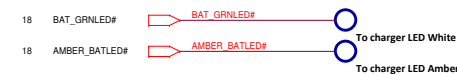
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Connect to SB



Charger LED

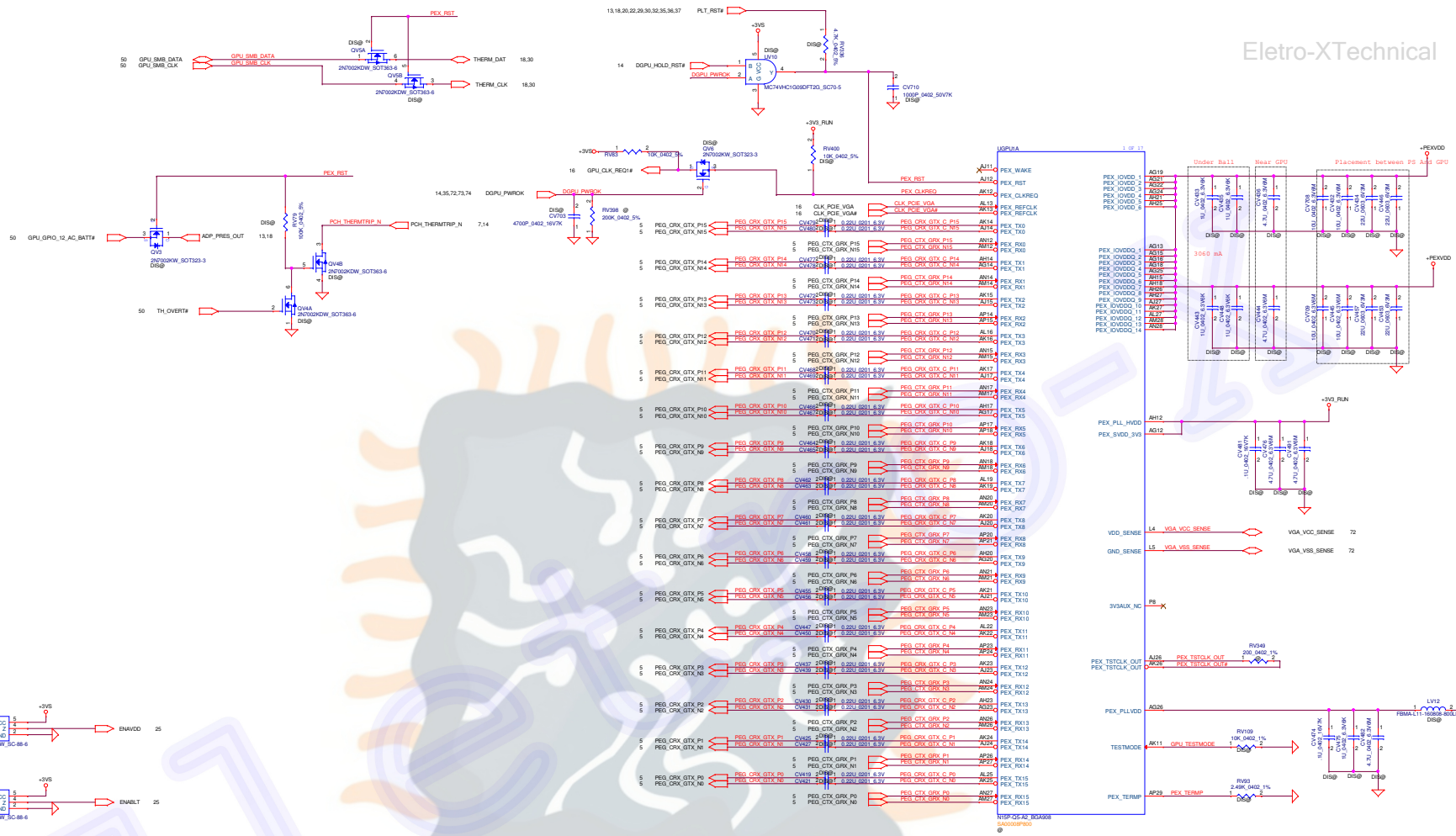


Eletro-XTechnical

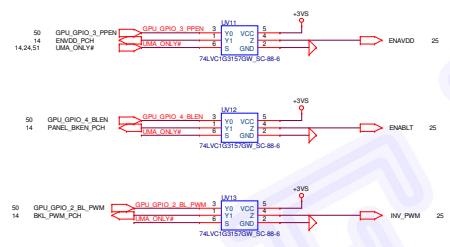
Eletro-X

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				Date	Thursday, November 19, 2015
				Sheet	39 of 80

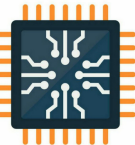


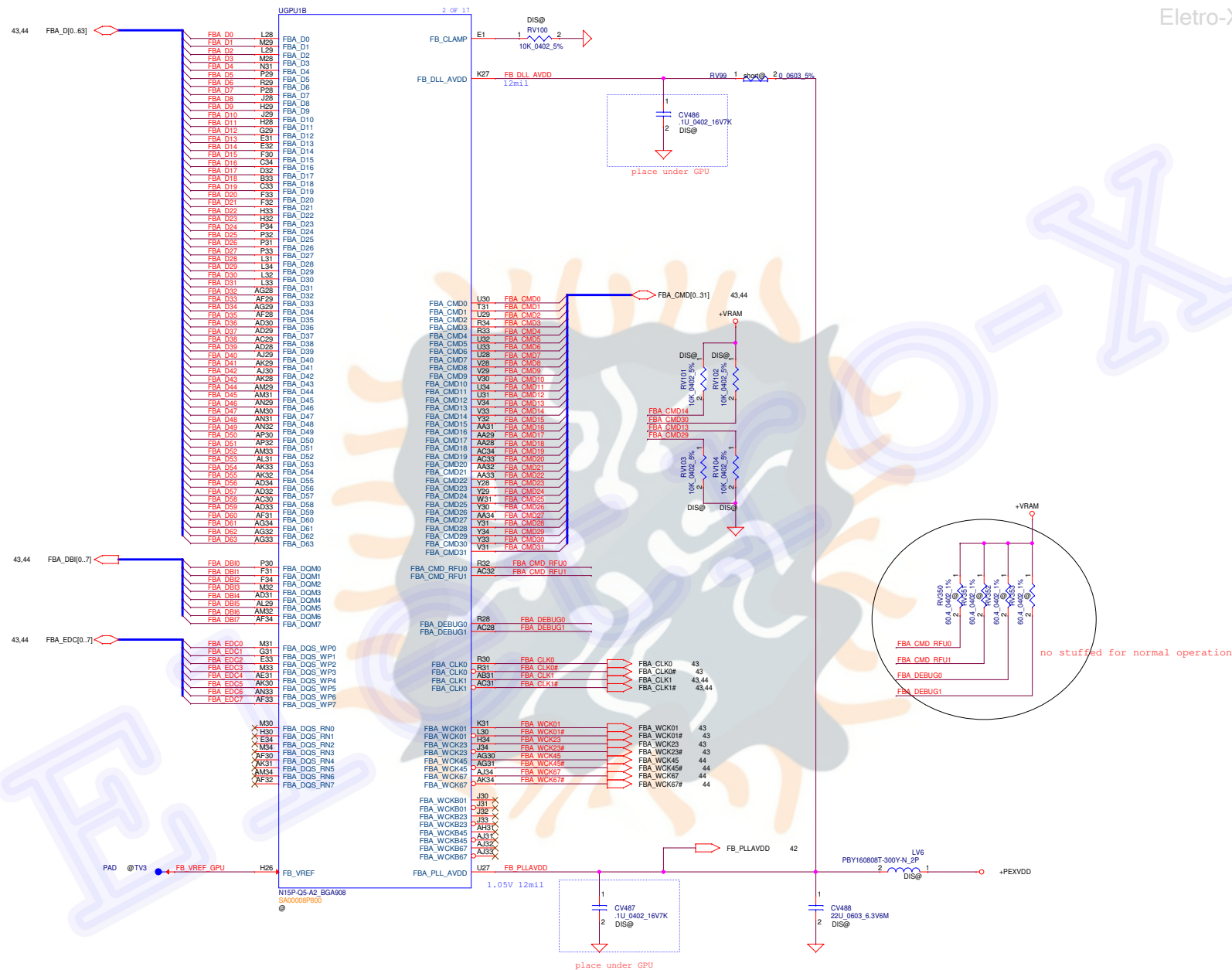


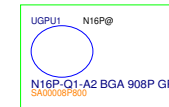
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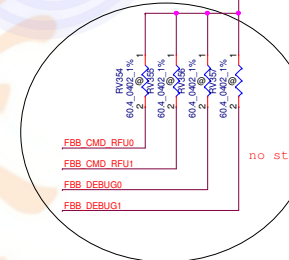
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<p>Author: Thursday, November 18, 2015</p>					







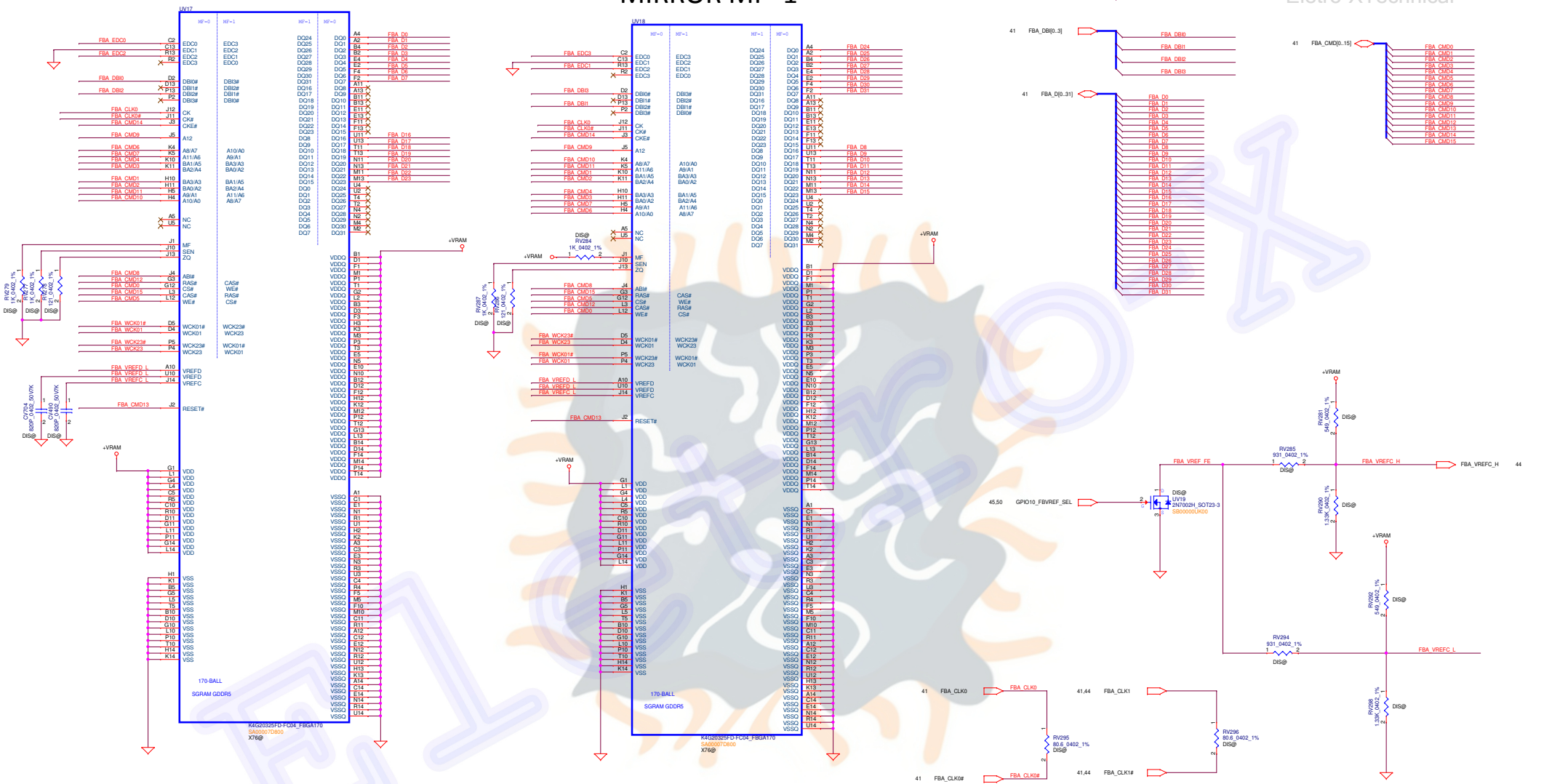
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	UV17, UV18, UV20, UV21, UV22, UV23, UV25, UV26	RV244
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X7663732L11		S2034200280
NH4G	Hynix S8000SV500 128MB2/2.5G M50C4824AJR-T2C FBGA	34.8K
X7663732L12		S2034348280



no stuffed for normal operation

NORMAL MF=0

MIRROR MF=1

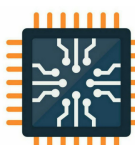


Eletron-XTechnical

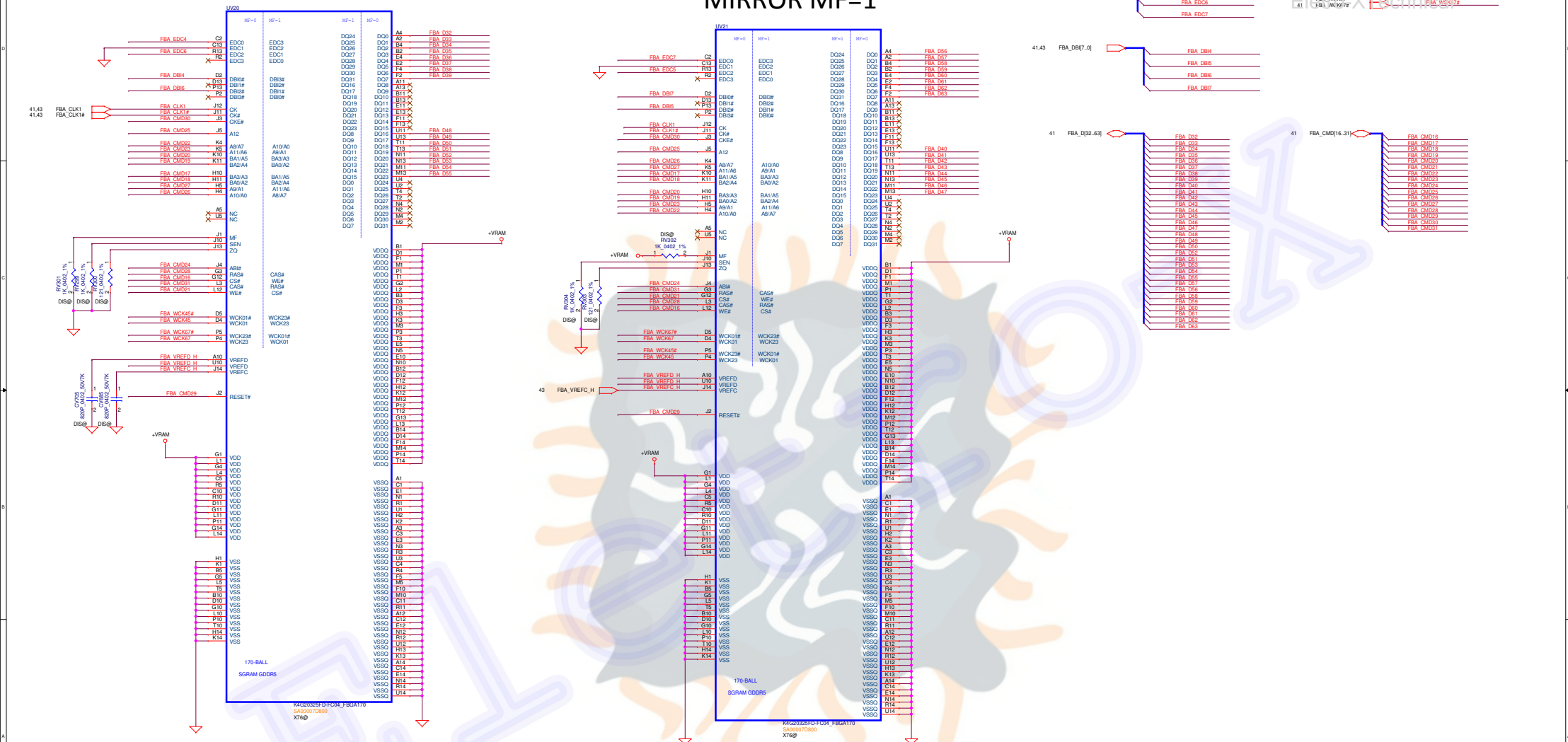
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Date	Monday, November 16, 2015	Sheet	43	of	80

Eletron-XTechnical

Eletron-X



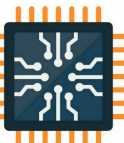
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2012/03/23		2012/12/31		PARTITION A (63..32)	
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				Document Number	1.0
Date:				Monday, November 16, 2015	
				Sheet	44 of 80

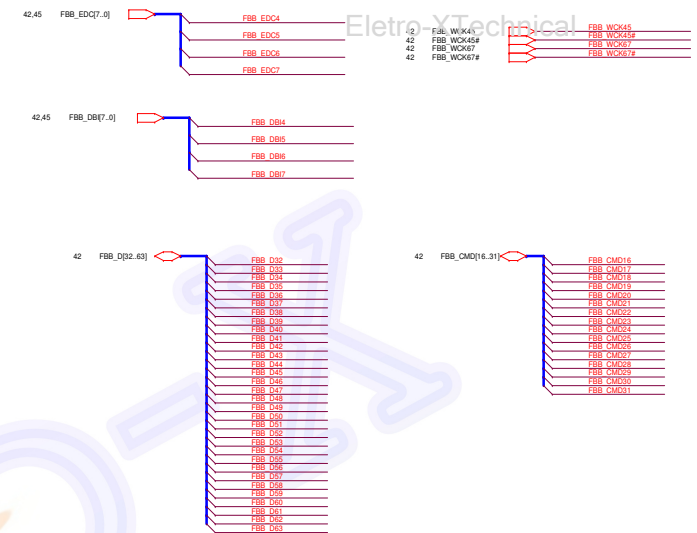
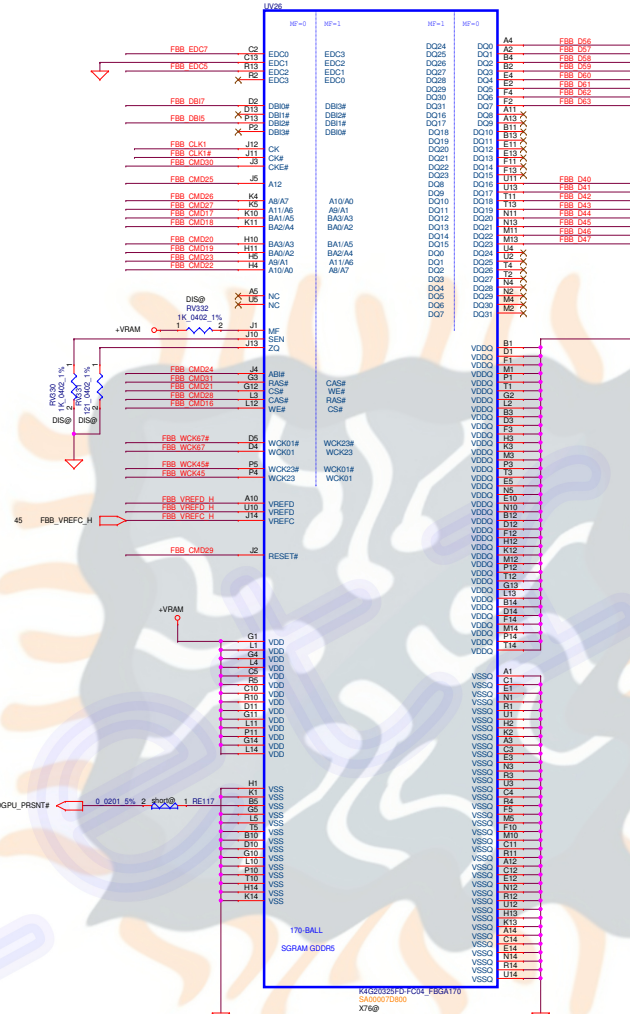


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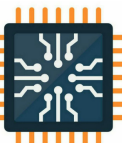


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Monday, November 16, 2015 10:01 AM			Deleted All All	

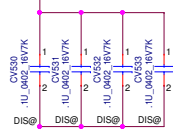
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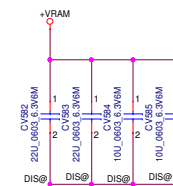
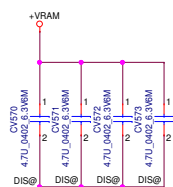
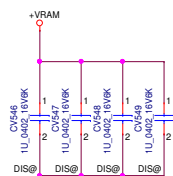
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				46	10
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Place under GPU

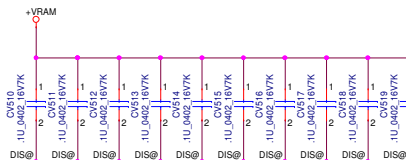
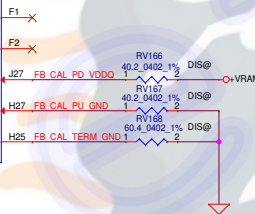
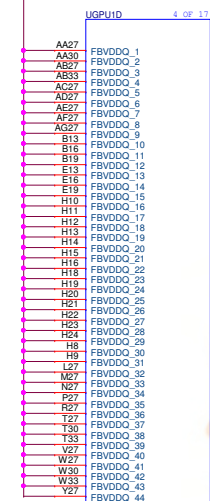


Close to GPU
Place close to GPU as option if there is space

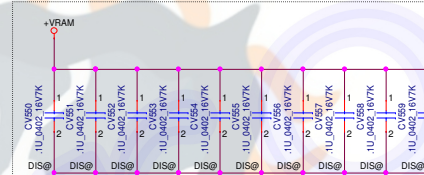
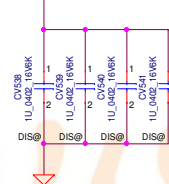


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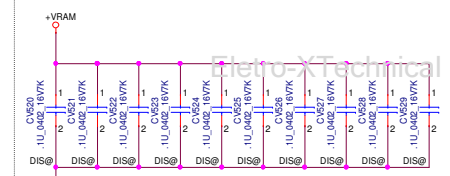
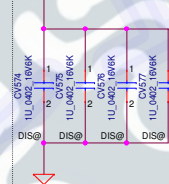
+VRAM



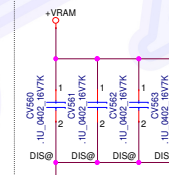
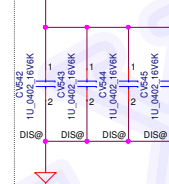
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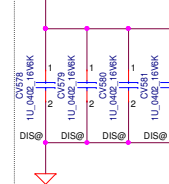
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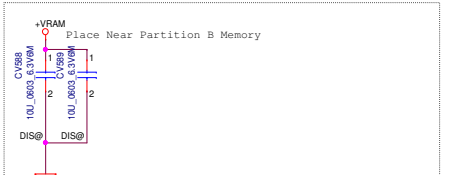
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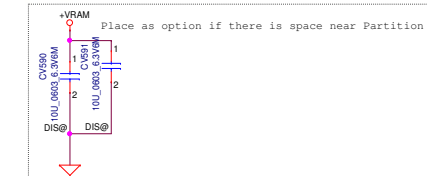
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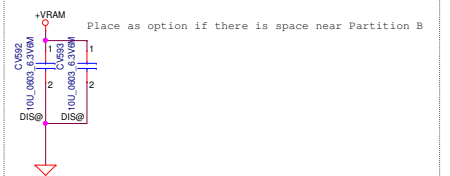
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Place Near Partition B Memory

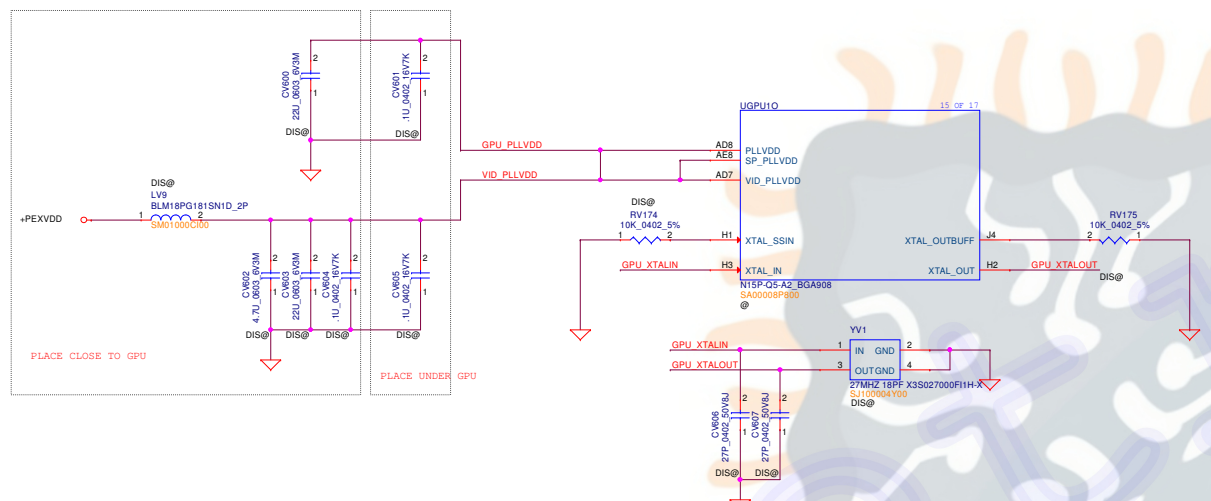
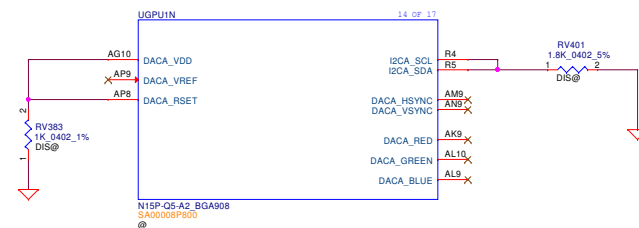


Place as option if there is space near Partition A

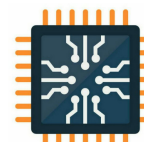


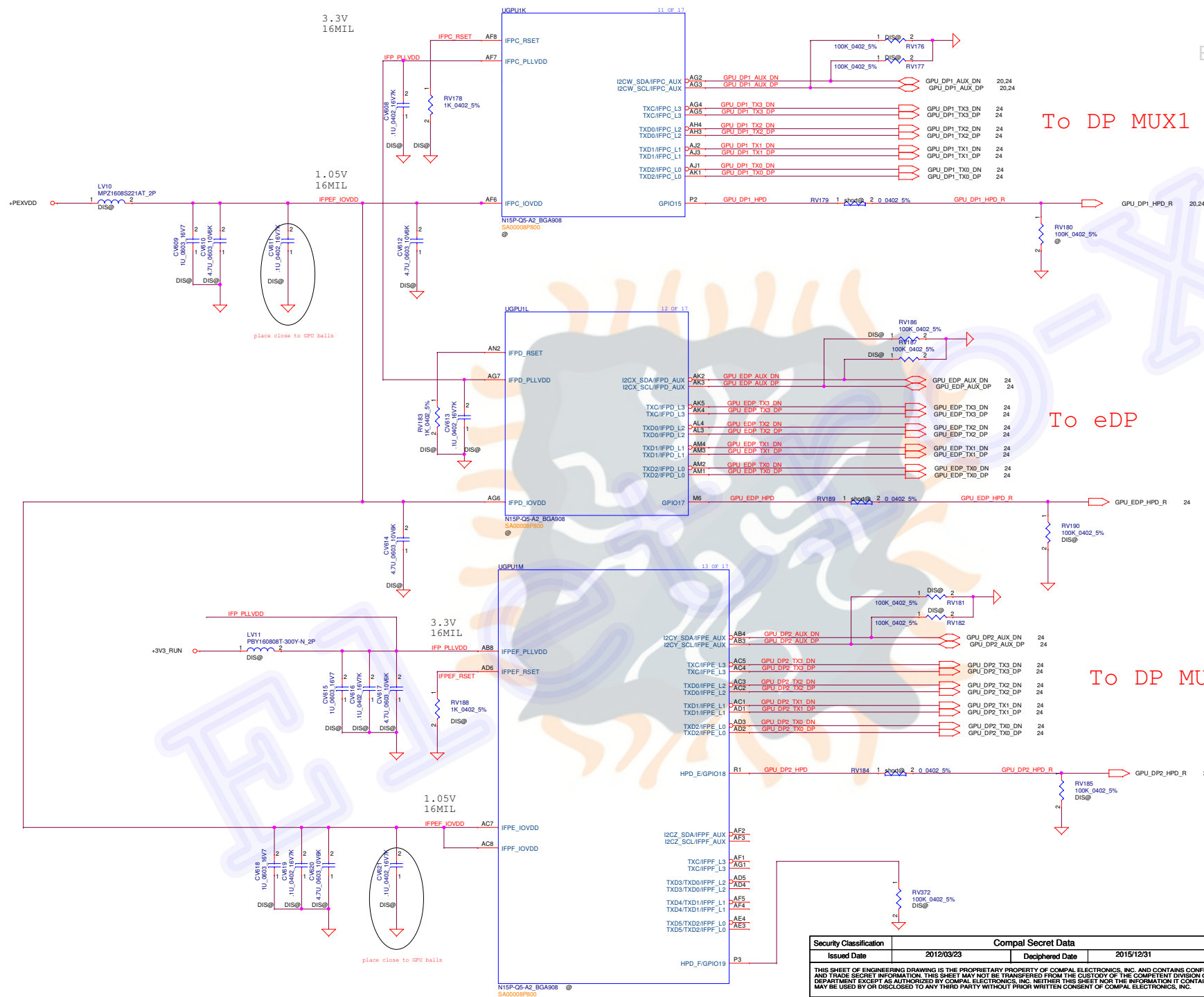
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Issued Date	2012/03/23	Deciphered Date	2015/12/31	Title	SACA PILL, CRYSTAL	
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				Custom		
Date:	Monday, November 16, 2015	Sheet	4A	of	80	



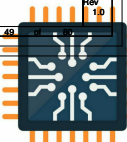


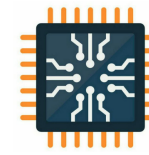
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To eDP

To DP MUX 2

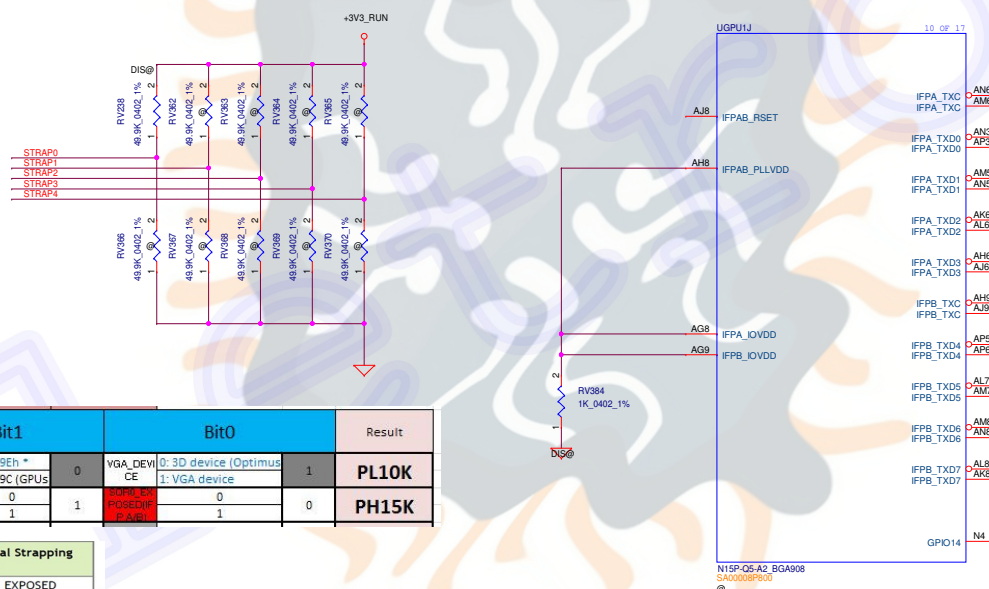
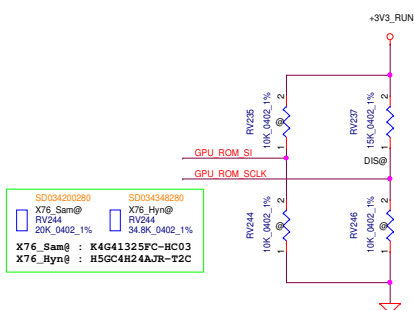
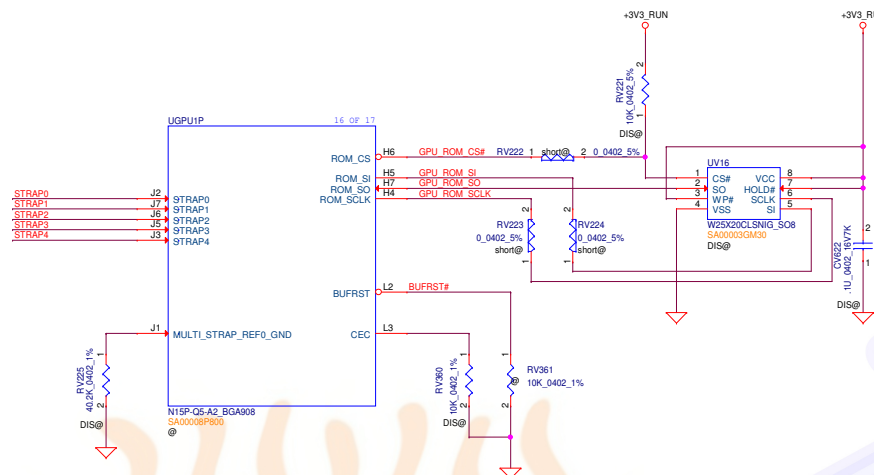
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Issued Date	2012/03/23	Deciphered Date	2015/12/31	Title	DP LINKS C,D
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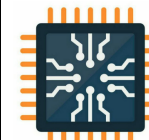
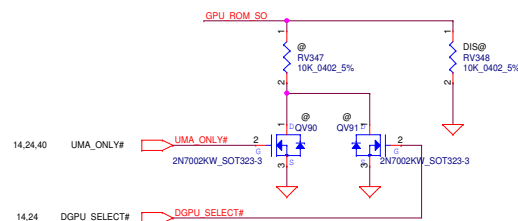


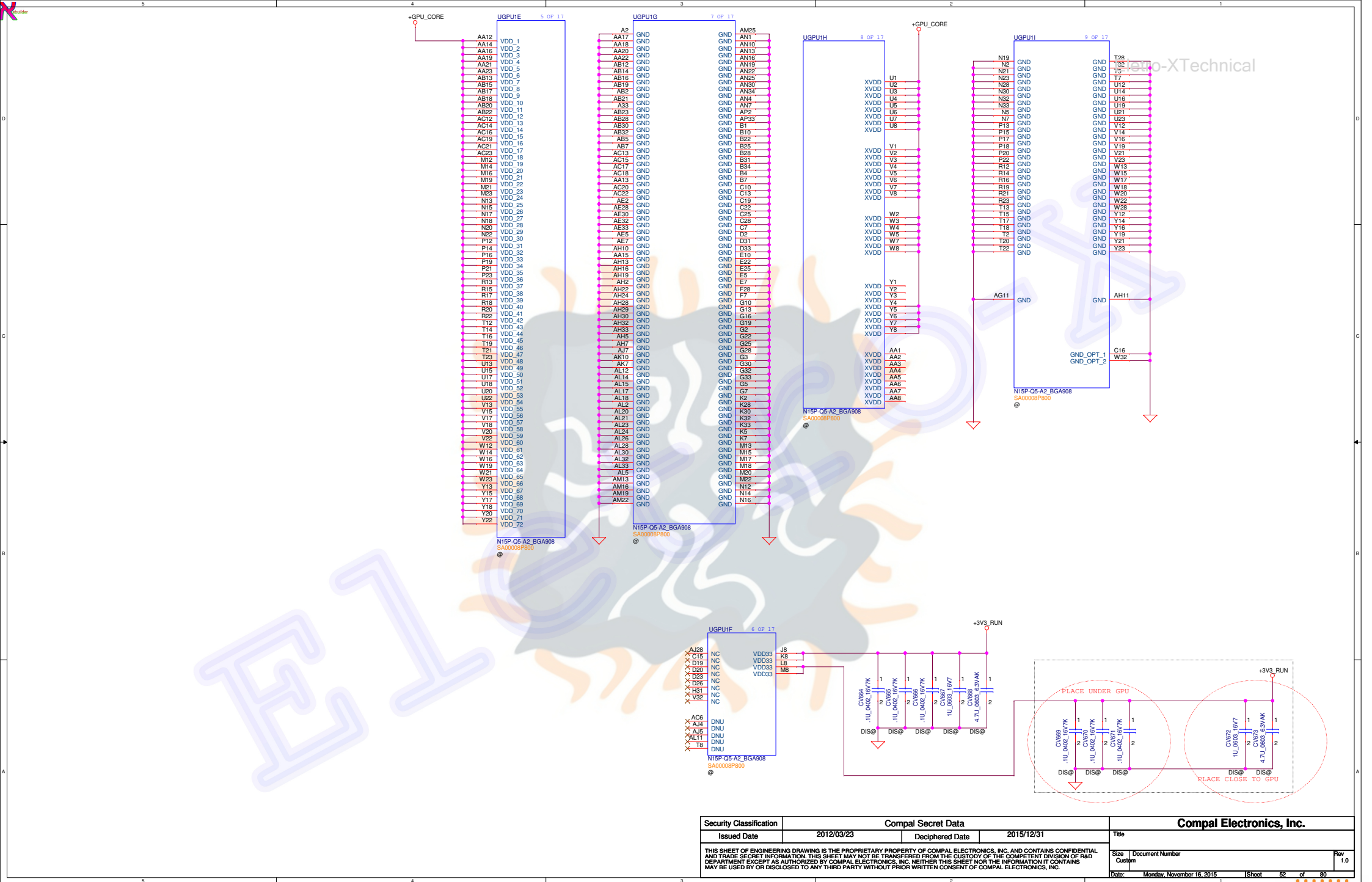
0000 4.99K to GND	1000 4.99K to VCC
0001 10K to GND	1001 10K to VCC
0010 15K to GND	1010 15K to VCC
0011 20K to GND	1011 20K to VCC
0100 24.9K to GND	1100 24.9K to VCC
0101 30.1K to GND	1101 30.1K to VCC
0110 34.8K to GND	1110 34.8K to VCC
0111 45.3K to GND	1111 45.3K to VCC

Function	Bringup Mode
RAMCFG[2]	ROM_SO
RAMCFG[1]	ROM_SI
RAMCFG[0]	STRAP3
3GIO_PADCFG_LUT_ADR[2]	STRAP2
3GIO_PADCFG_LUT_ADR[1]	STRAP1
3GIO_PADCFG_LUT_ADR[0]	STRAP0
SMB_ALT_ADDR	ROM_SCLK
PCIE_MAX_SPEED	STRAP4

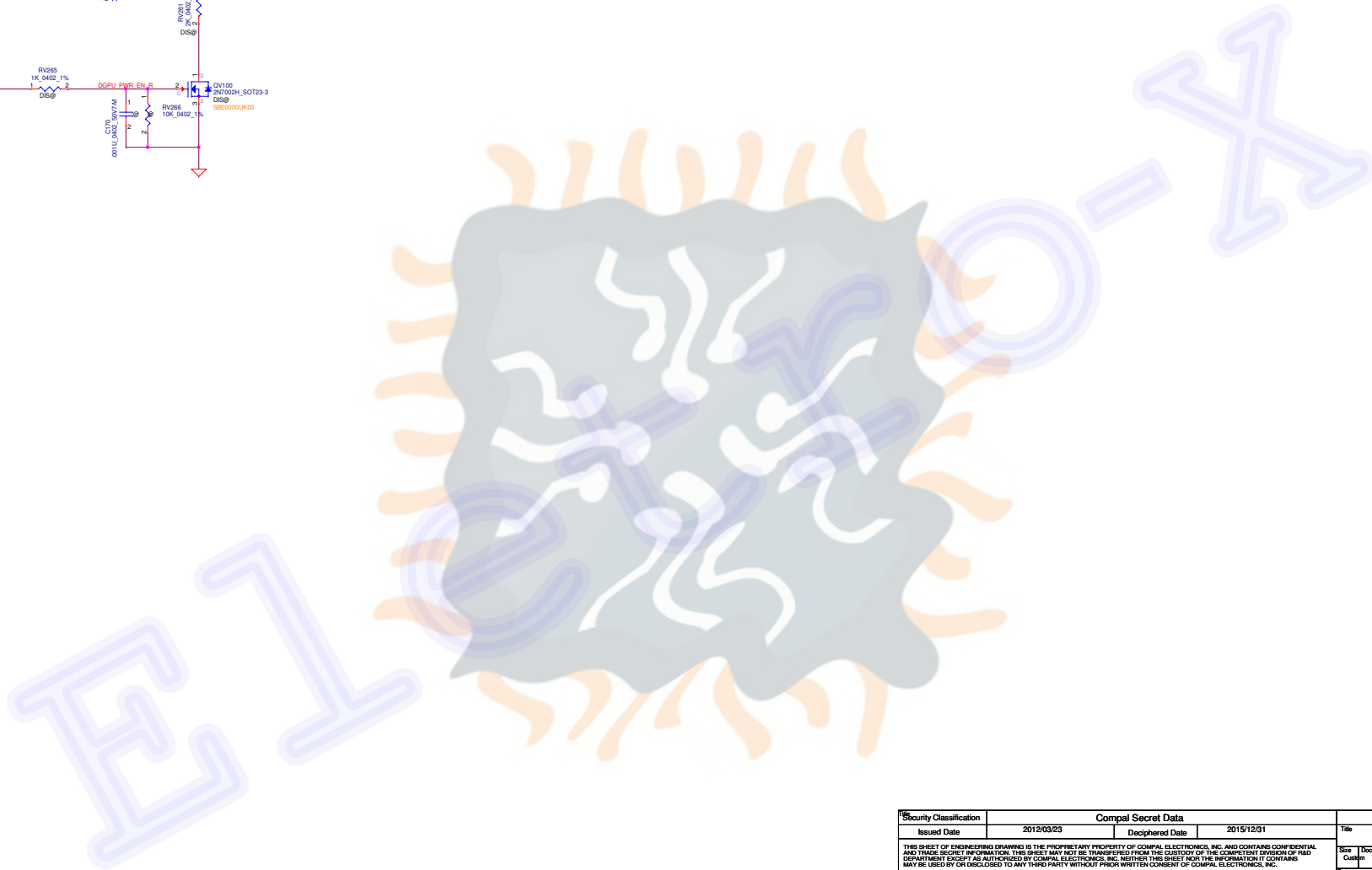
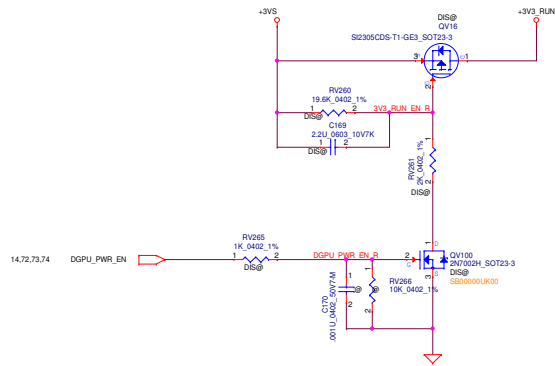


Strap Pin Name	Logical Strapping Bit 0	Logical Strapping Bit 1	Logical Strapping Bit 2	Logical Strapping Bit 3
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SORO_EXPOSED
ROM_S1	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Strapp 49 kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			
STRAP2				
STRAP3				
STRAP4				



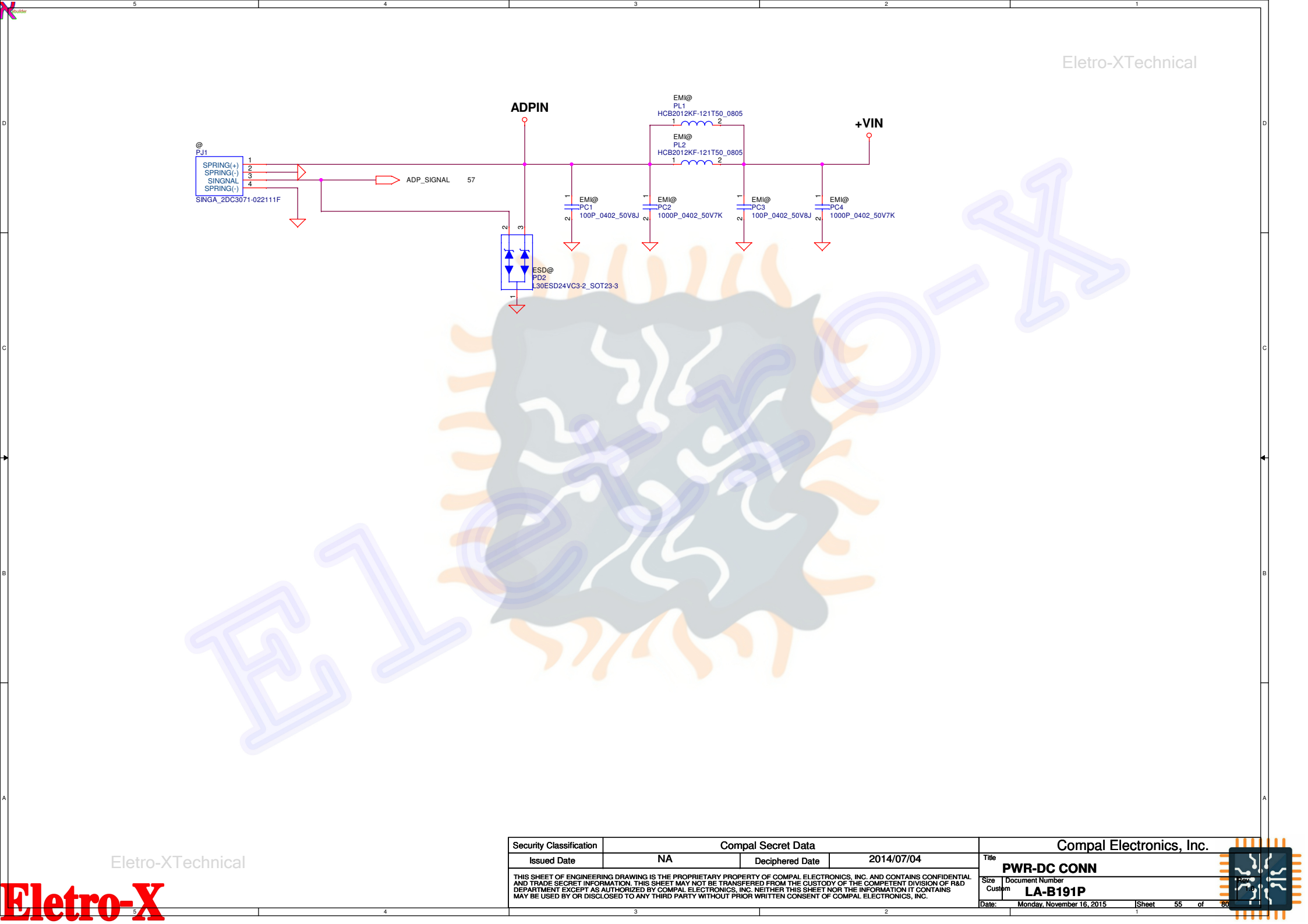


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52		of		80	



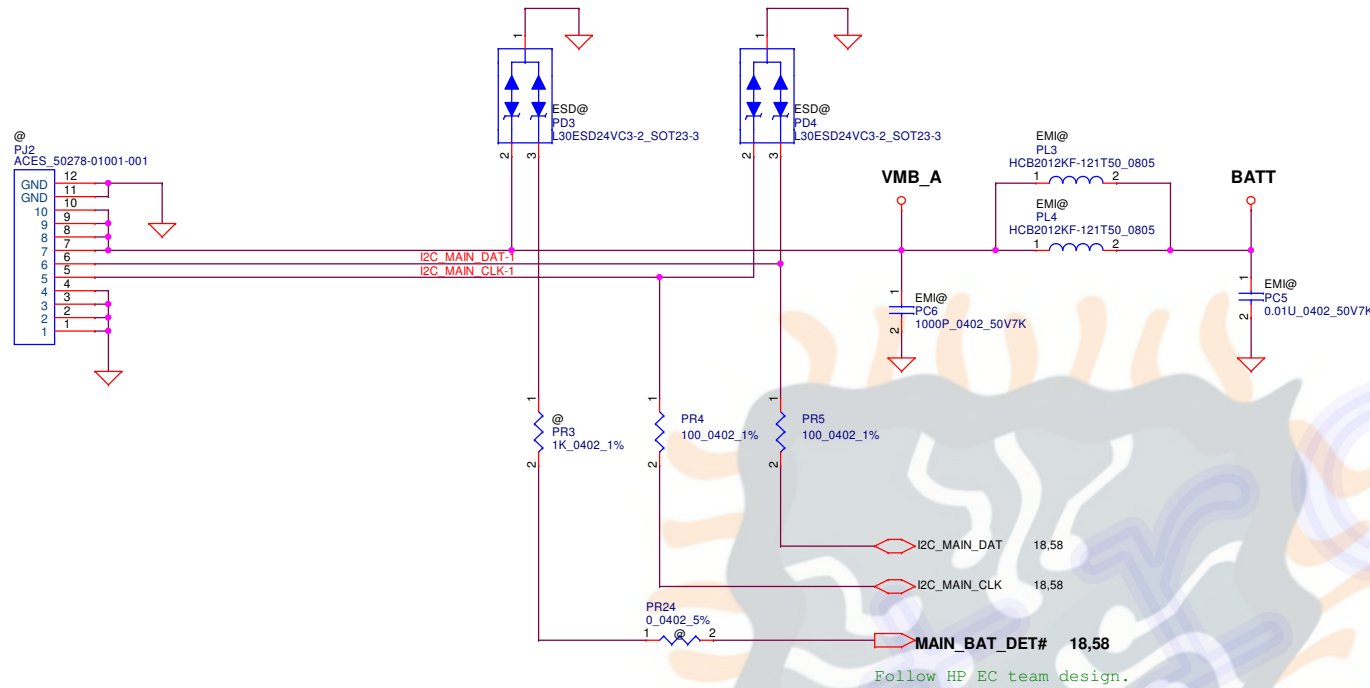
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Size	Document Number	Rev			
Creation		1.0			
Date	Monday, November 16, 2015	Sheet	53	of	80





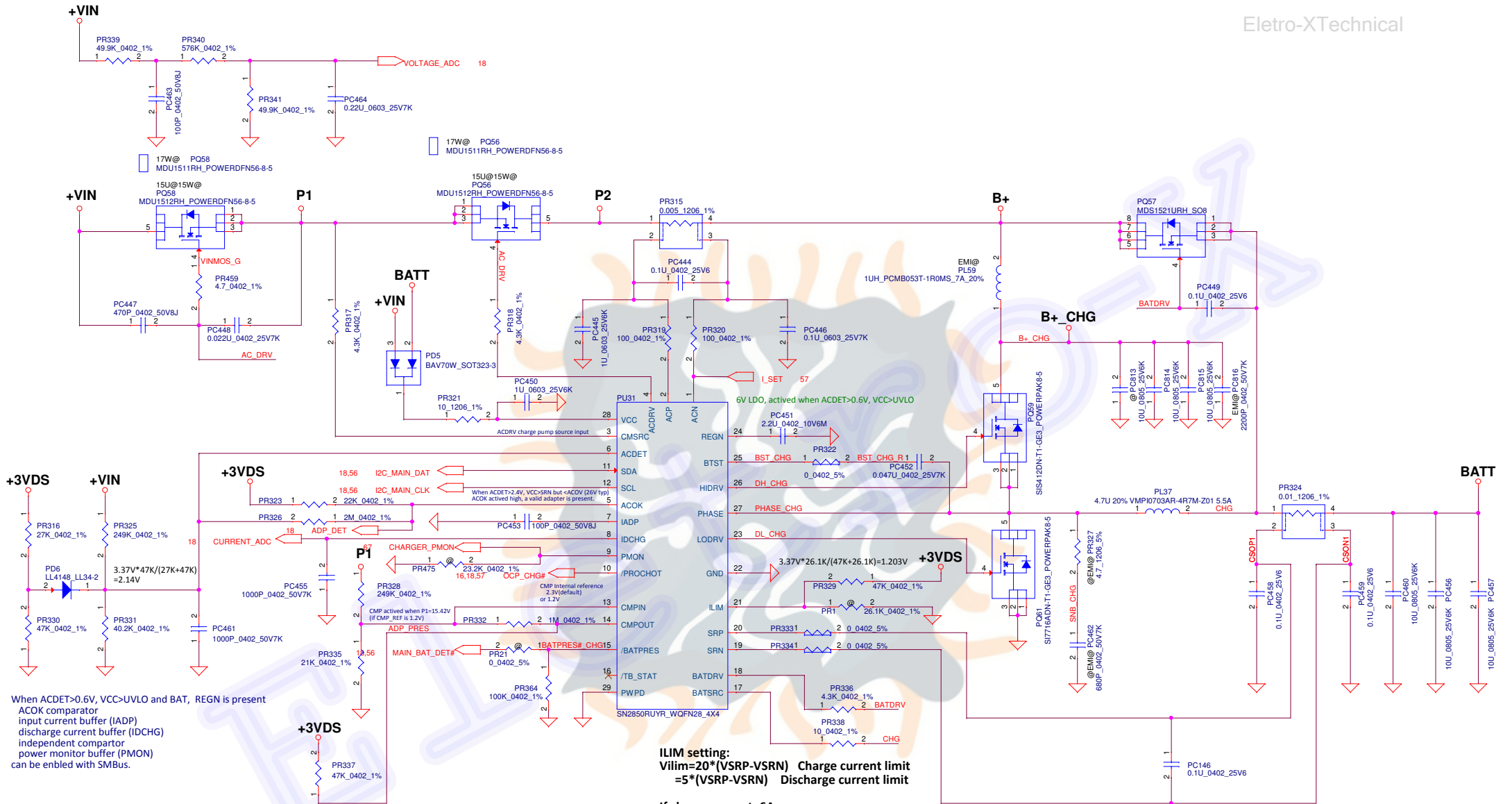
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				Custom	LA-B191P
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	NA	Deciphered Date	2014/07/04	Title	PWR-BATT CONN
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When ACDET>0.6V, VCC>UVLO and BAT, REGN is present
ACOK comparator (IADP)
discharge current buffer (IDCHG)
independent comparator
power monitor buffer (PMON)
can be enabled with SMBus.

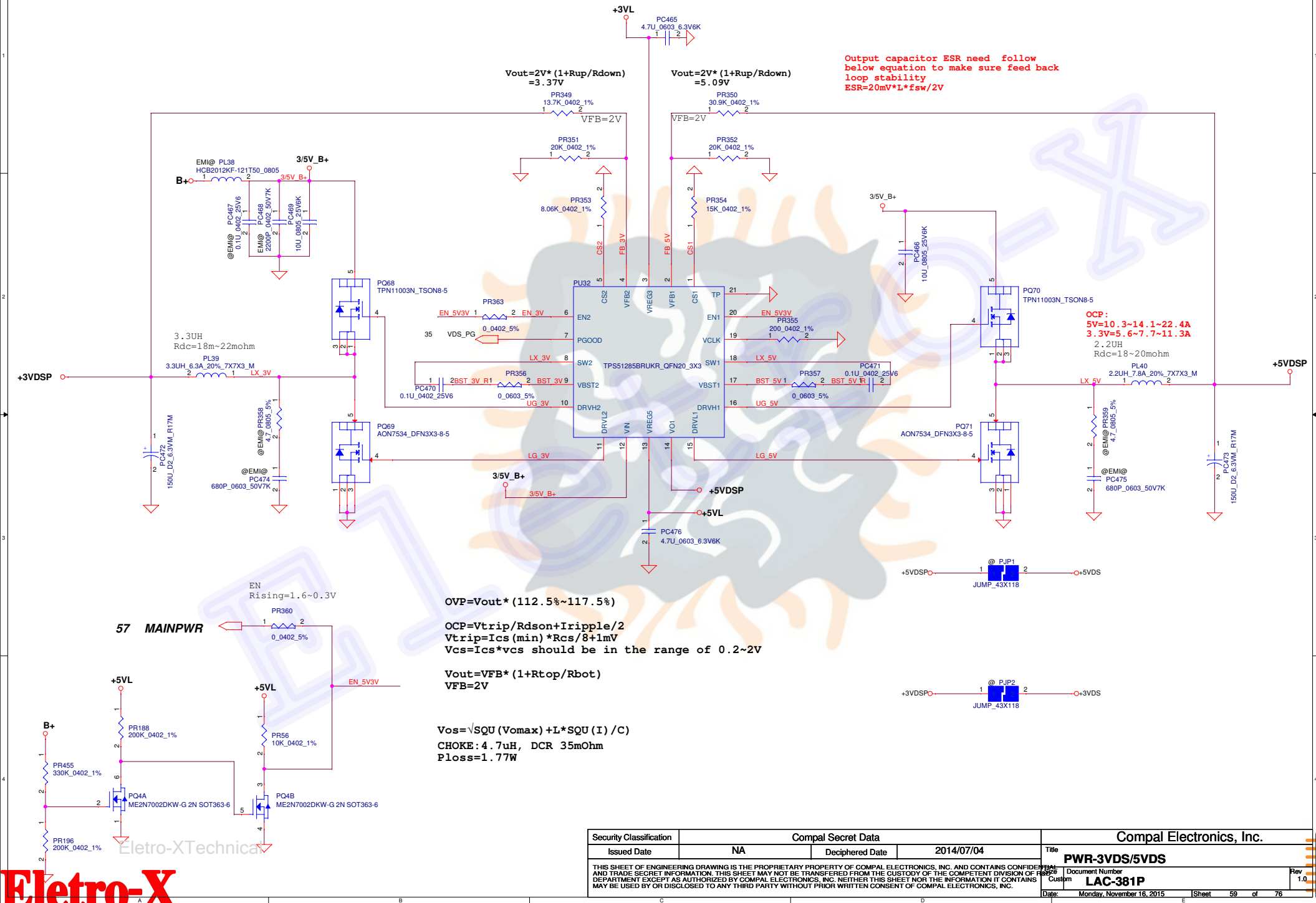
When adapter is present, the PROCHOT# function is enabled by the below bits.
When adapter is removed, ICRT, INOM, BATPRES, and ACOK functions are automatically disabled in the PROCHOT profile.
Comparator, IDCHG, and VSYS function settings are preserved.
When all the bits are 0, PROCHOT# function is disabled.

- Bit 6: CMPOUT, independent comparator output (CMPOUT pin HIGH to LOW)
0: disable (default at POR); 1: enable
- Bit 5: ICRT, adapter peak current
0: disable; 1: enable (default at POR)
- Bit 4: INOM, adapter average current (105% of input current limit)
0: disable (default at POR); 1: enable
- Bit 3: IDCHG, battery discharge current
0: disable (default at POR); 1: enable
- Bit 2: VSYS, system voltage on SRN for 2s - 4s battery
0: disable (default at POR); 1: enable
- Bit 1: BATPRES#, upon battery removal (BATPRES# pin LOW to HIGH)
0: disable (default at POR); 1: enable (one-shot rising edge triggered)
- Bit 0: ACOK, upon adapter removal (ACOK pin HIGH to LOW)
0: disable (default at POR); 1: enable (one-shot falling edge triggered)

ILIM setting:
Vilim=20*(VSRP-VSRN) Charge current limit
=5*(VSRP-VSRN) Discharge current limit

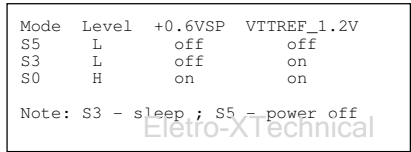
If charge current=6A,
Vilim=20*(6A*0.01ohm)
=1.2V

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				Date:	Monday, November 16, 2015
				Sheet	58

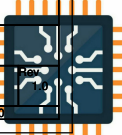


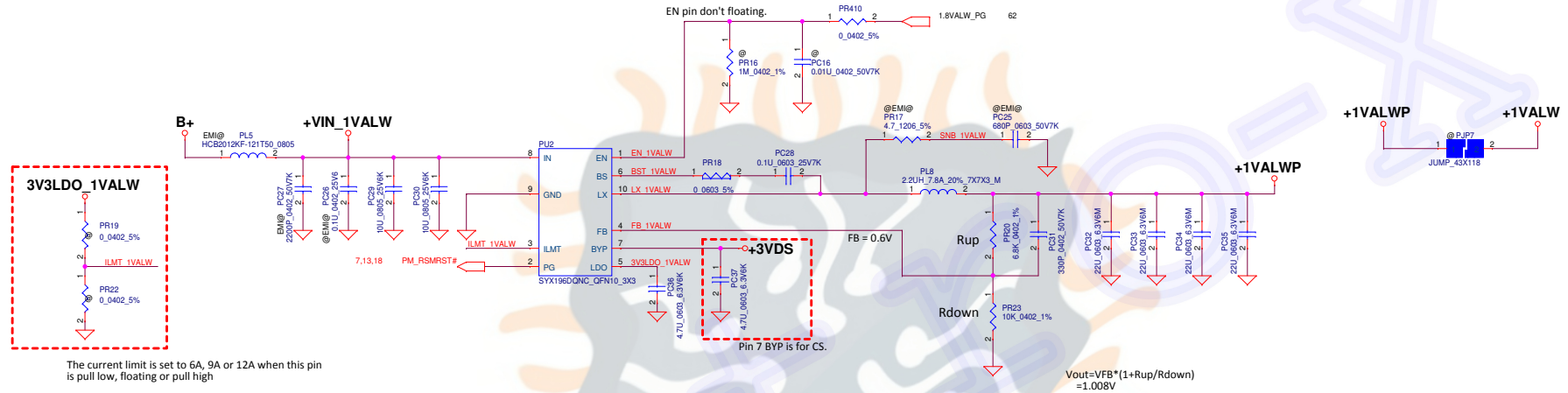
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Issued Date	NA	Deciphered Date	2014/07/04	Title	PWR-3VDS/5VDS
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				Rev	1.0
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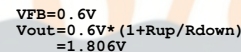




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Title	PWR-1.0VALW		
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MODE=GND (VCCIO)
 MODE=Float (VCCPCH)
 MODE=100Kohm to GND (EDRAM/EOPIO)
 MODE=150Kohm to GND (Others)

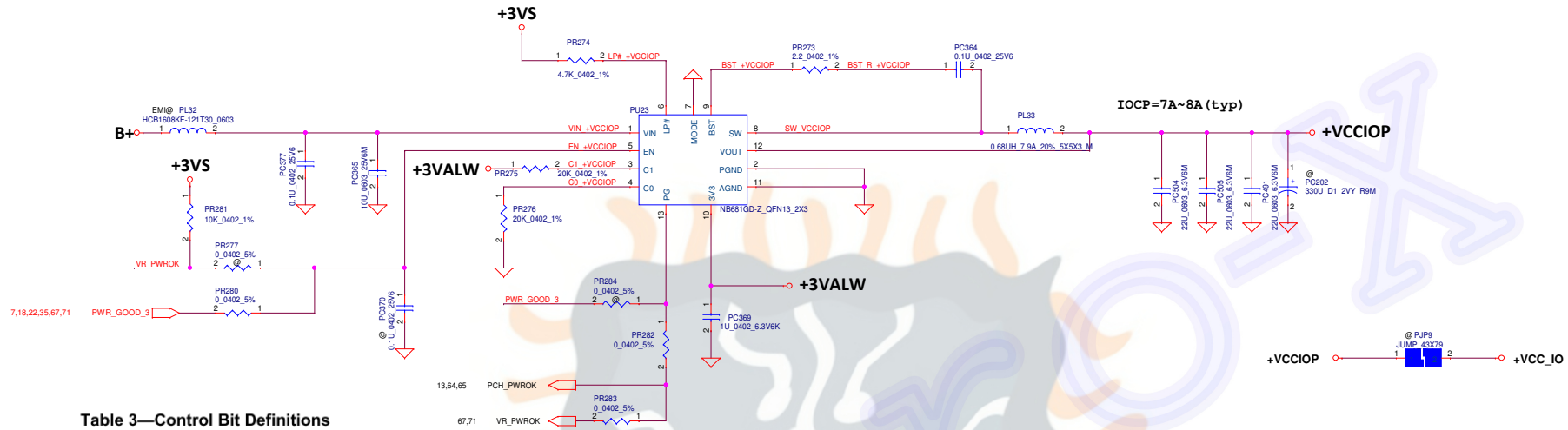


Table 3—Control Bit Definitions

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPCH	0	X	X	0.7
	1	0	0	0.8
	1	0	1	0.85
	1	1	0	0.9
	1	1	1	0.95
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2



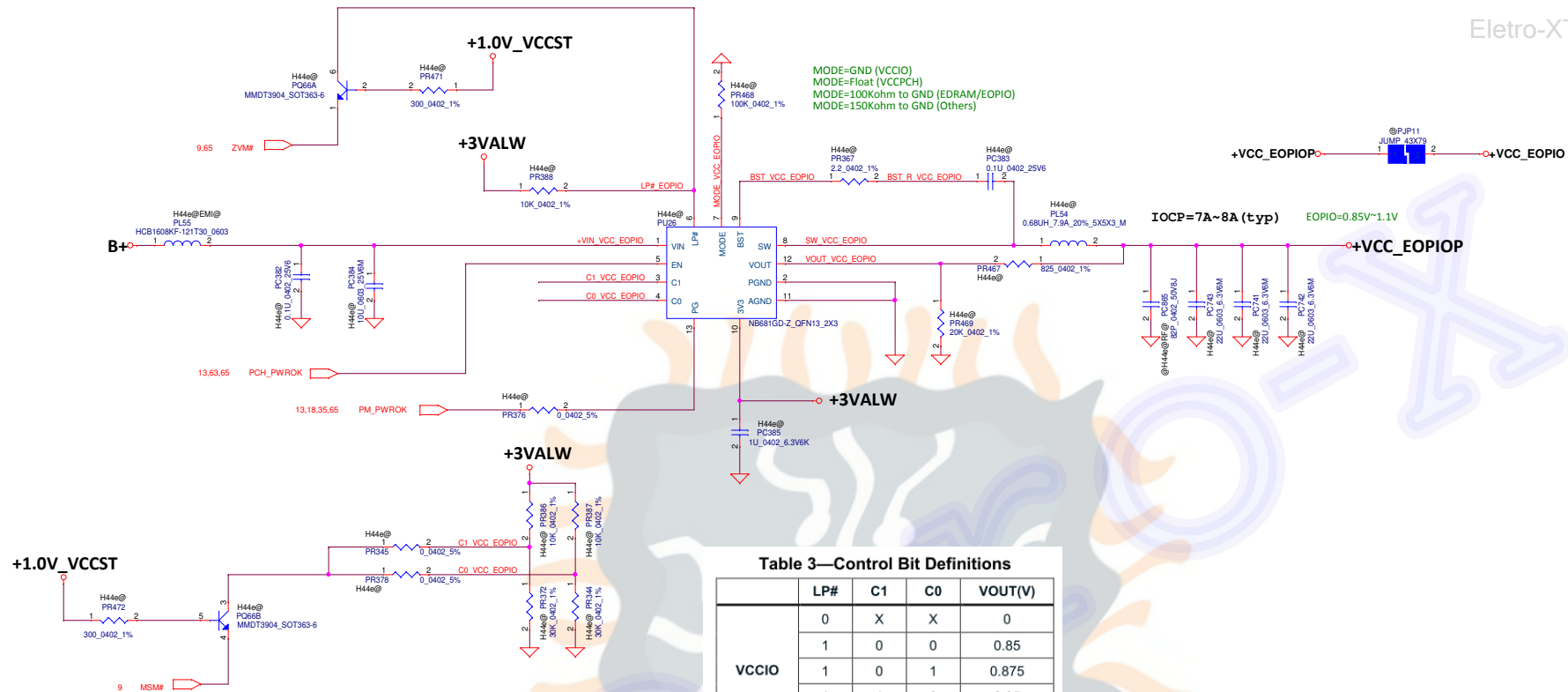


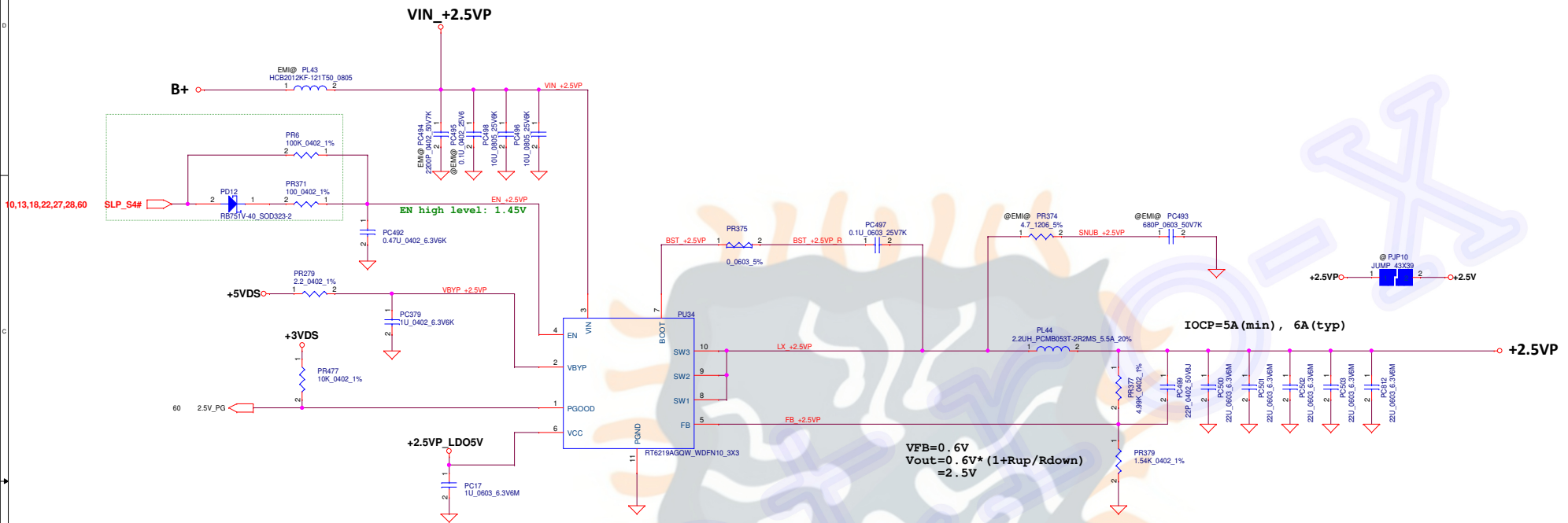
Table 3—Control Bit Definitions

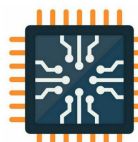
	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPCH	0	X	X	0.7
	1	0	0	0.8
	1	0	1	0.85
	1	1	0	0.9
	1	1	1	0.95
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

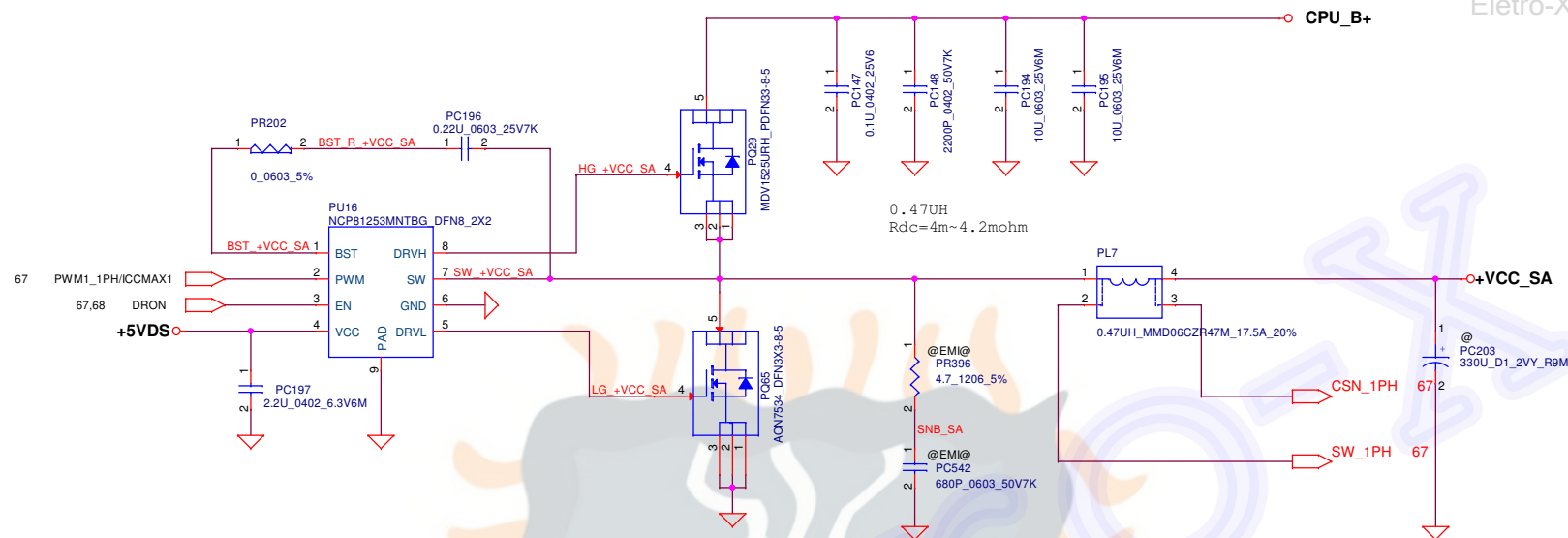




	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPCH	0	X	X	0.7
	1	0	0	0.8
	1	0	1	0.85
	1	1	0	0.9
	1	1	1	0.95
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

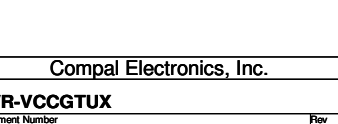
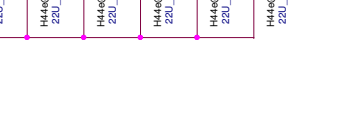
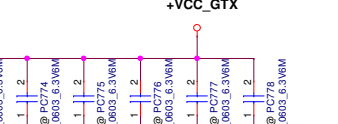
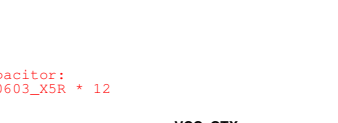
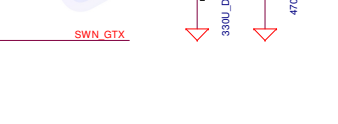
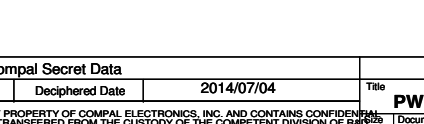
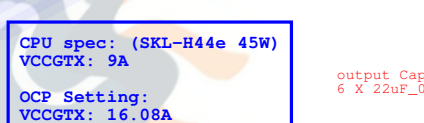
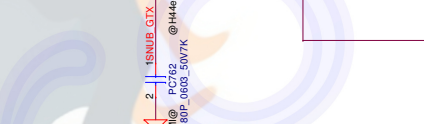
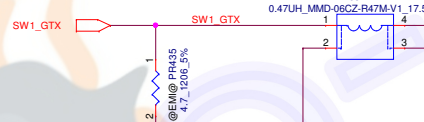
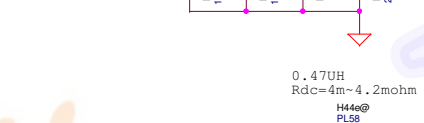
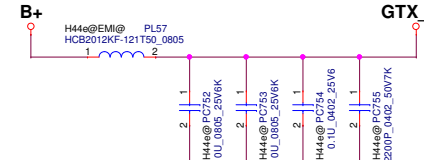
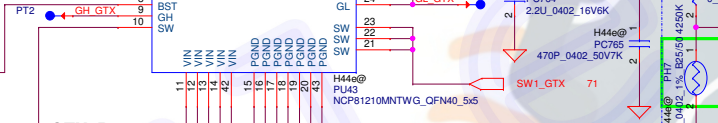
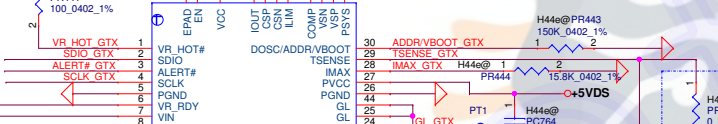
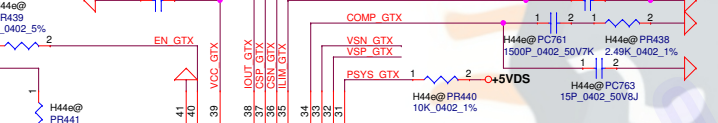
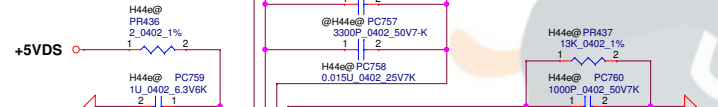
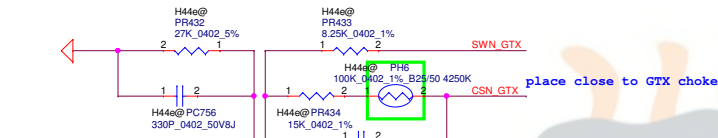
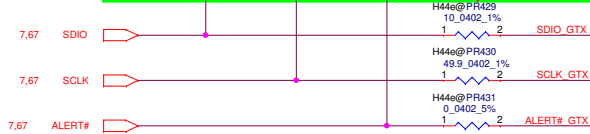
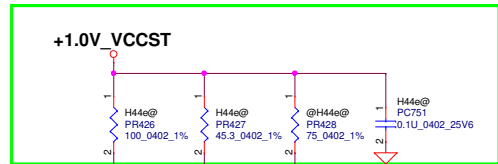






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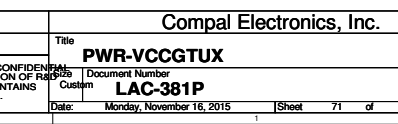
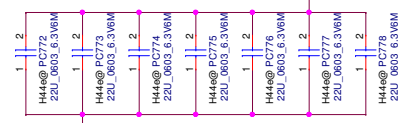
It depend on NCP81206 or NCP81210 close to CPU will be unpop.



CPU spec: (SKL-H44e 45W)
VCCGTX: 9A
OCP Setting:
VCCGTX: 16.08A

output Capacitor:
6 X 22uF_0603_X5R * 12

+VCC GTX



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$$V_{boot} = V_{ref} \cdot R_{ref2} / (R_{ref1} + R_{ref2} + R_{boot})$$

$$R_t = R_{refadj} // (R_{boot} + R_{ref2})$$

$$V_{min} = V_{ref} \cdot [R_{ref2} / (R_{ref2} + R_{boot})] \cdot [R_t / (R_{ref1} + R_t)]$$

$$V_{max} = V_{ref} \cdot R_{ref2} / [(R_{ref1} / R_{refadj}) + R_{boot} + R_{ref2}]$$

$$V_{out} = V_{min} + N \cdot V_{step}$$

$$V_{step} = (V_{max} - V_{min}) / N_{max}$$

PWM-VID Spec and component Values

PWM-VID Spec	Config A	Config B	Config C
Vmin	0.6V	0.6V	0.65V
Vmax	1.2V	1.2V	1.15V
Vboot	0.875V	0.9V	0.9V
Voltage step	6.25mV	6.25mV	25mV
N of Voltage level	96	96	20
Rrefadj PR913	39K	20K	39K
Rref1 PR915	39K	20K	30K
Rboot PR930	1.5K	2K	3K
Rref2+PR914+PR904	30K	18K	24K
Crefin PC940	1.5K	0	3K
	1.5nf	2.7nf	1.8nf

Module model information

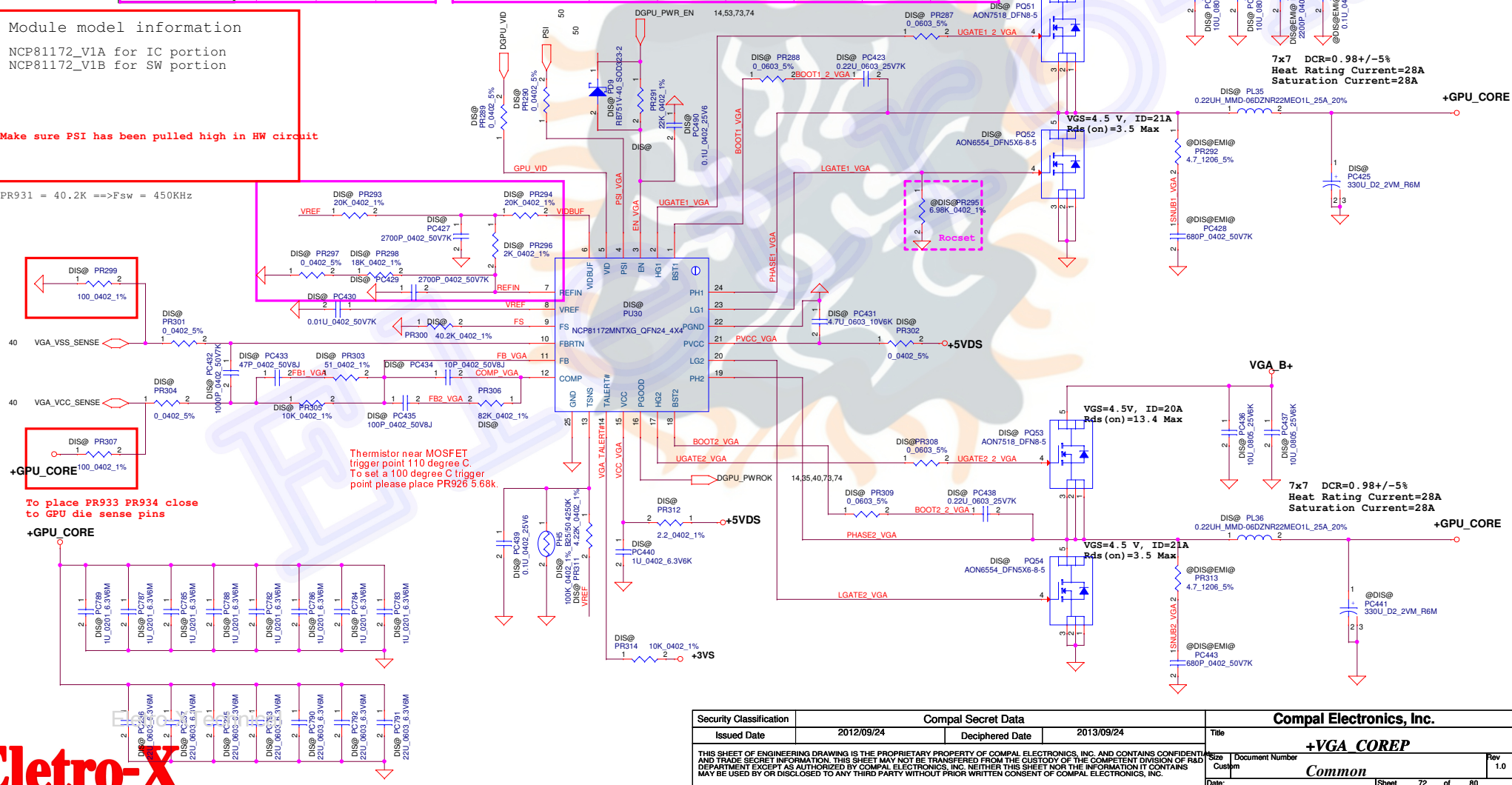
NCP81172_V1A for IC portion
NCP81172_V1B for SW portion

Make sure PSI has been pulled high in HW circuit

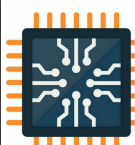
PR931 = 40.2K ==> F_{sw} = 450KHz

Different VGA Chip (different EDP-Peak Current) need select different solution

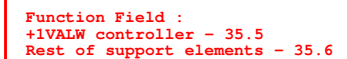
VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B
Rated TDP Power at T _J =102C	18W	25W	18W	13W	18.9W	25W
Boosted GPU Total at T _J =102C	25W	32W	25W	20W	23W	N/A
EDP-Continuous at T _J =102C	24A	32A	26A	22A	25A	27A
EDP-Peak at T _J =102C	35A	55A	45A	35A	35A	40A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A
OCP Setting Current	42A	66A	54A	42A	42A	48A
Roset (PR911)	6.98K	@	21K	6.98K	6.98K	6.98K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L
Polymer Cap	560U	4.5mohm	4.5mohm	4.5mohm	4.5mohm	4.5mohm
Or OSCON	330U	9mohm	9mohm	9mohm	9mohm	9mohm
	560U	10mohm	10mohm	10mohm	10mohm	10mohm
	390U	10mohm	10mohm	10mohm	10mohm	10mohm



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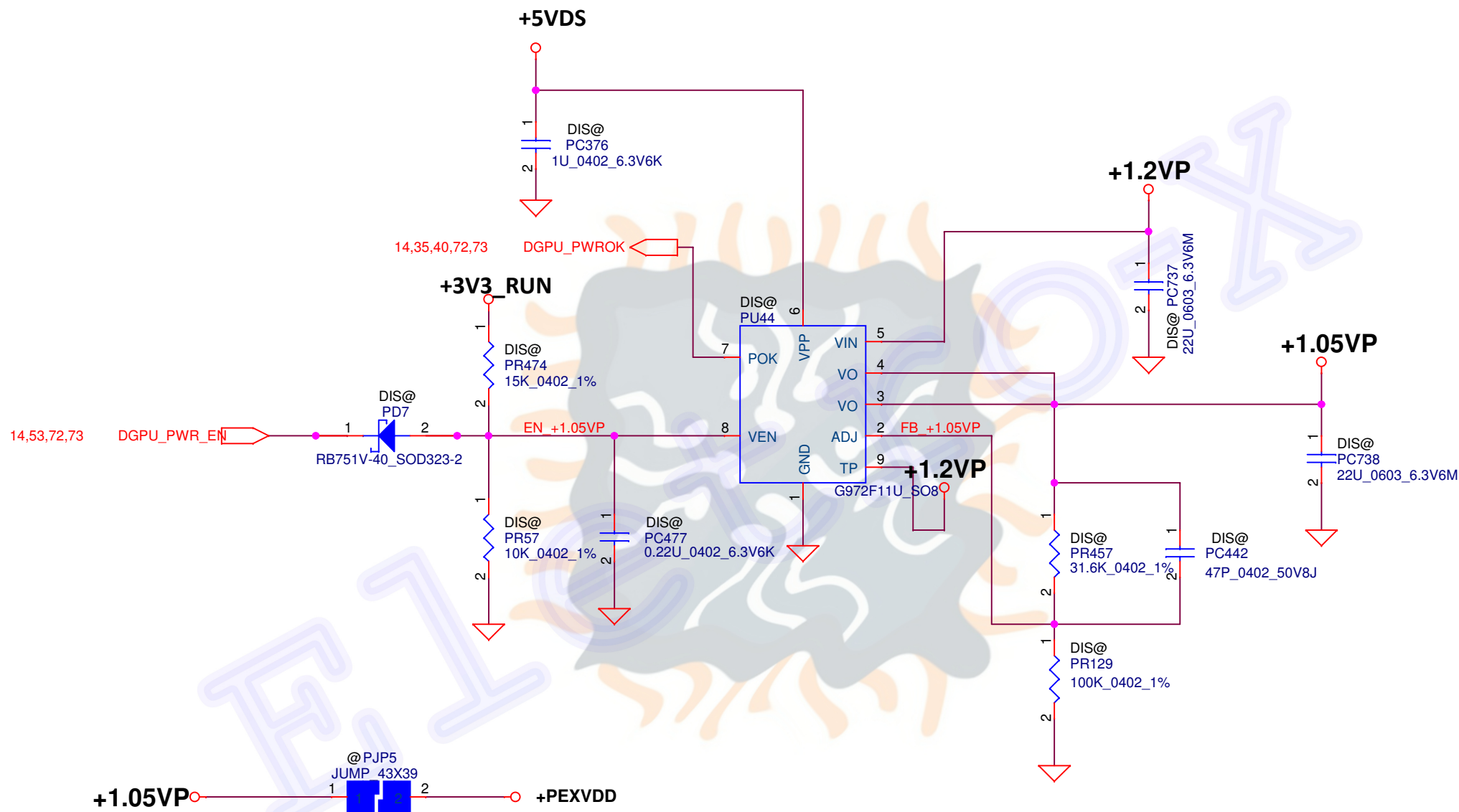


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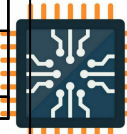


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				Size	Document Number
				AAX05	
Date	Monday, November 16, 2015			Sheet	73 of 80

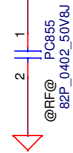




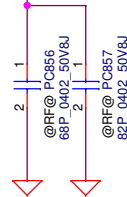
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Date: Monday, November 16, 2015 Sheet 74 of 80		



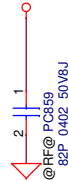
DDR_B+



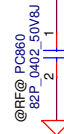
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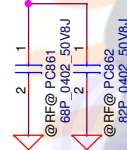
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VIN_+2.5VP

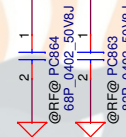


+2.5VP

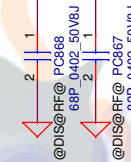


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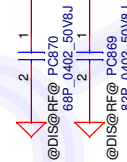
3/5V_B+



VIN_+VRAMP

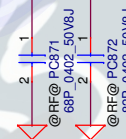


VGA_B+

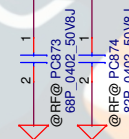


3/23 Add

B+



+VIN_VCC_OPC_EDRAM

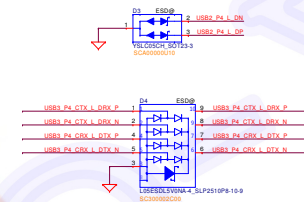
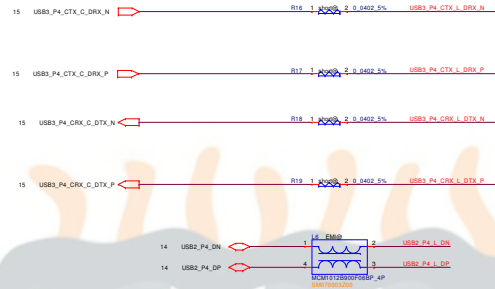
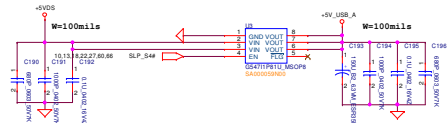


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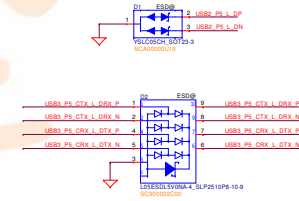
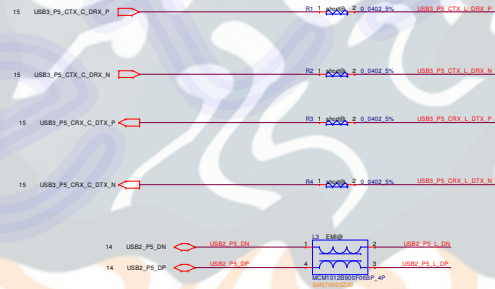
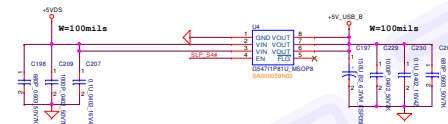
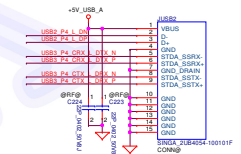


MB_USB 3.0 Without charger function

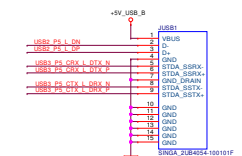
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USB3.0 / USB2.0 Port4 (Left Side)



USB3.0 / USB2.0 Port5 (Right Side)

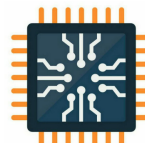
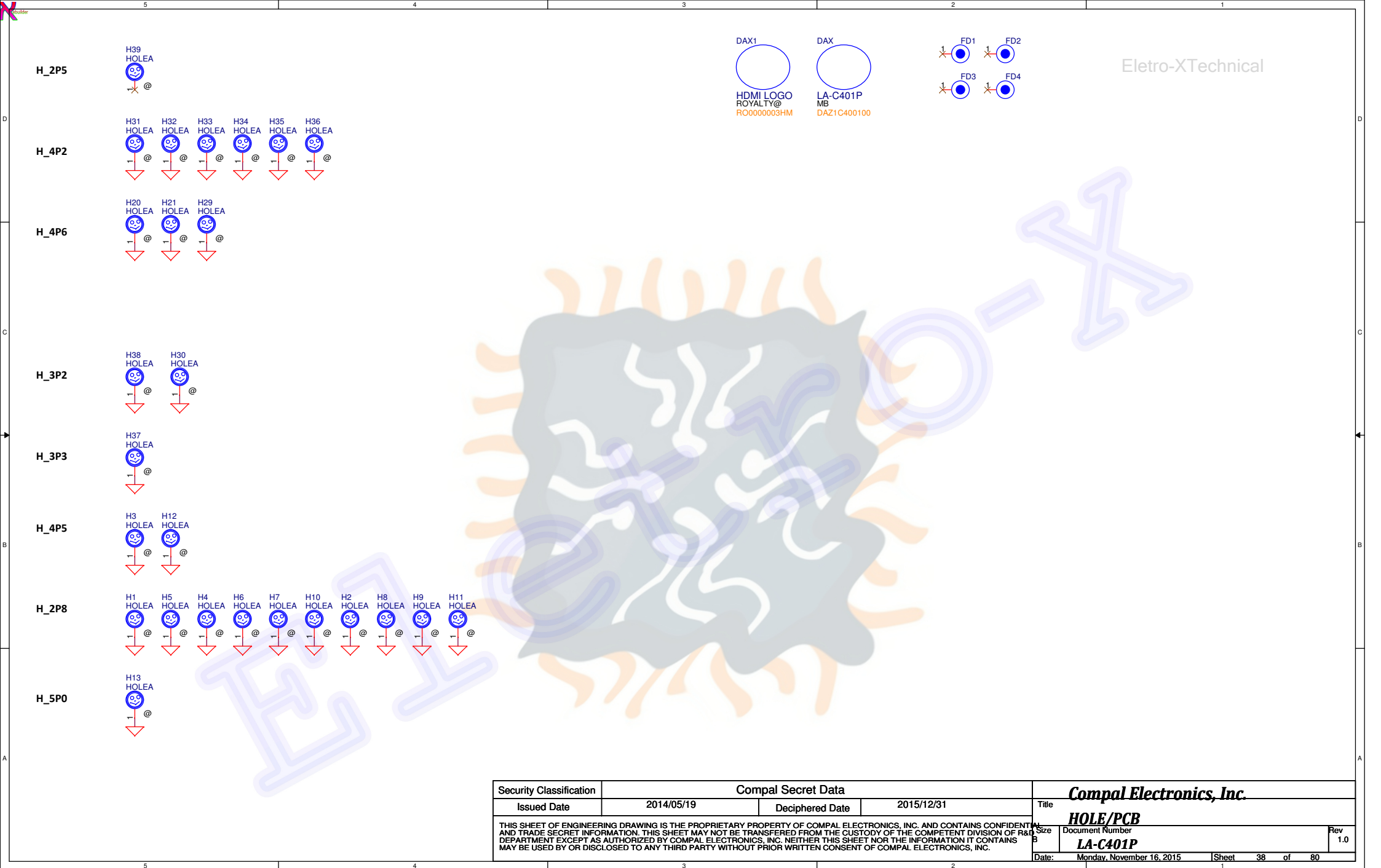


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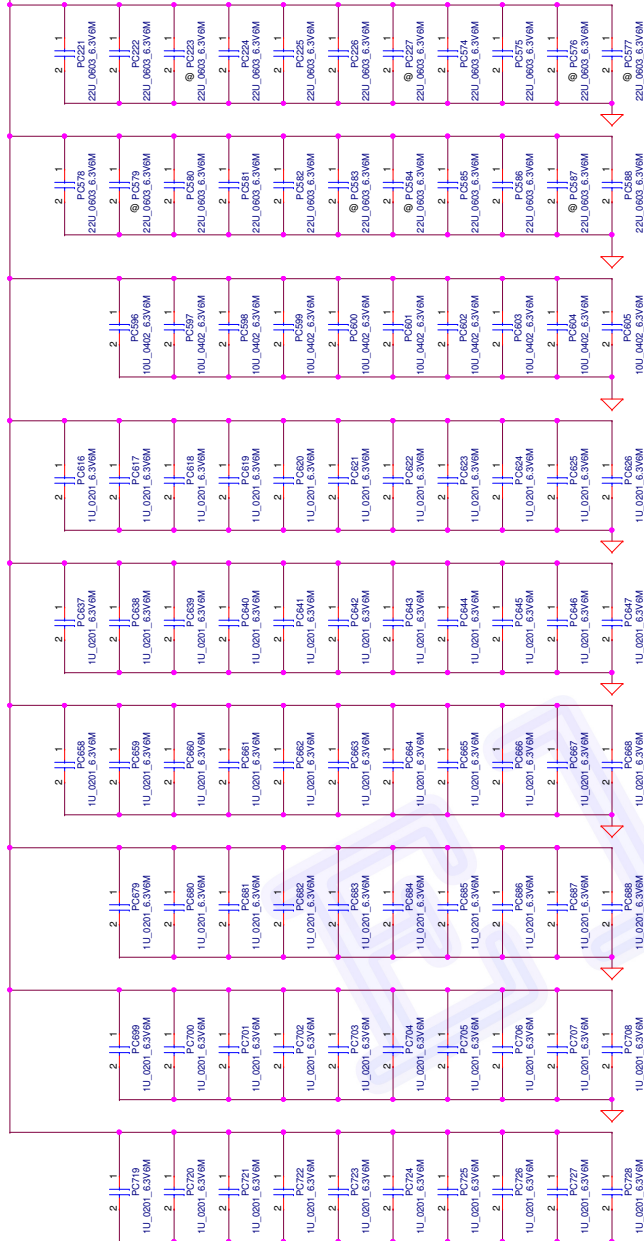




+VCC_CORE

Total VCCORE Output Capacitor:
 9 X 330uF
 32 X 22uF_0603_X5R
 63 X 1uF_0201
 10 X 10uF_0402

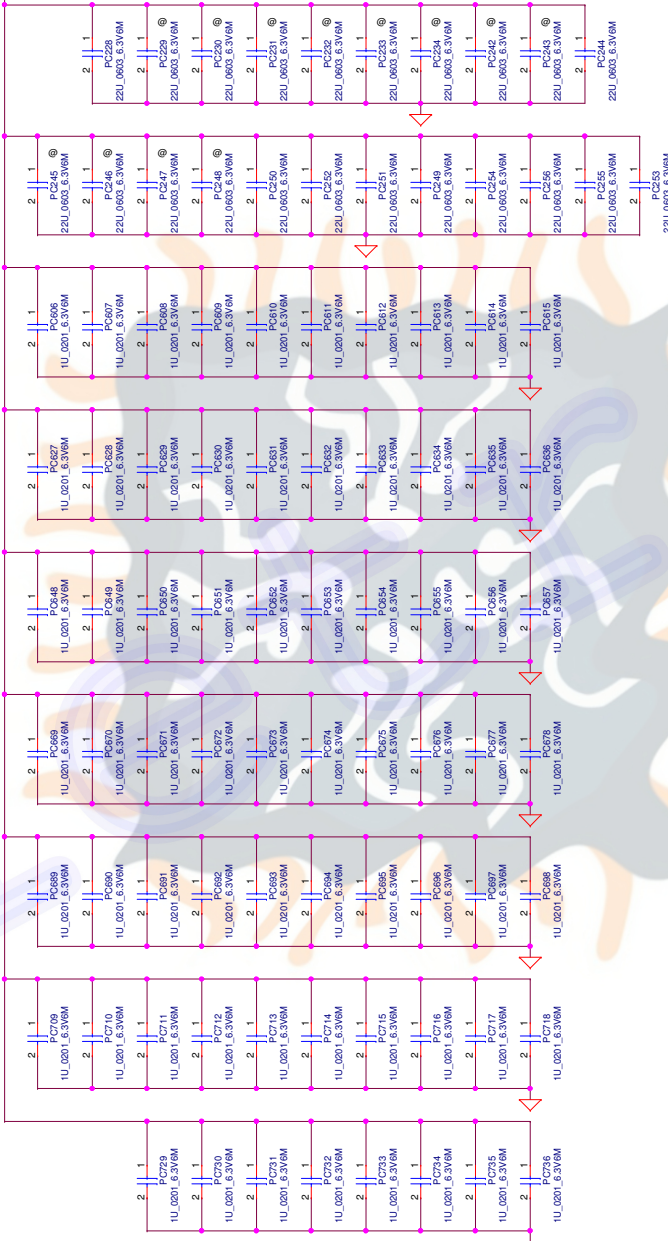
+VCC_CORE



+VCC_GT

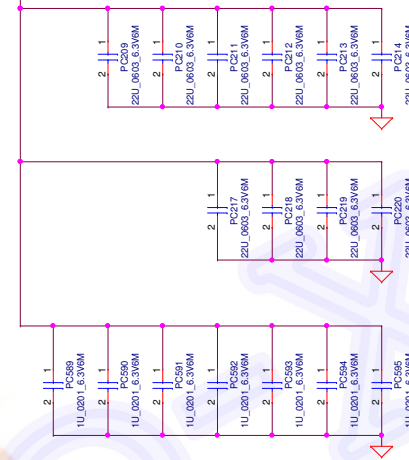
Total VCCGT Output Capacitor:
 2 X 330uF
 10 (+4) X 22uF_0603_X5R
 68 X 1uF_0201

+VCC_GT



+VCC_SA

Total VCCSA Output Capacitor:
 12 X 22uF_0603
 7 X 1uF_0201

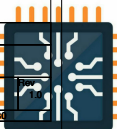


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							PWR-PROCESSOR DECOUPLING	
							Size	
							Custom	
							LA-B191P	
							Date:	
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Install below X63 level BOM structure for ver. 0.1

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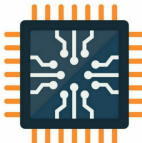
Un-pop parts BOM structure

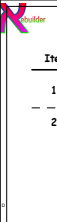
- @ : reserve, un-pop on all sku
- @DIS@: Discrete sku parts, un-pop
- @DIS@EMI@ : Discrete sku parts and belong to EMI parts, un-pop
- @EMI@ : EMI parts, un-pop
- @H44e@ : CPU H44e sku parts, un-pop
- @H44e@EMI@ : CPU H44e sku parts and belong to EMI parts, un-pop

Pop parts BOM structure

- DIS@: Discrete sku parts, pop
- DIS@EMI@ : Discrete sku parts and belong to EMI parts, pop
- EMI@ : EMI parts, pop
- ESD@ : ESD parts, pop
- H42@ : pop on CPU H42 sku only
- H44e@ : pop on CPU H44e sku only
- H44e@EMI@ : EMI parts, pop on CPU H44e sku only

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				Document Number	LA-B191P
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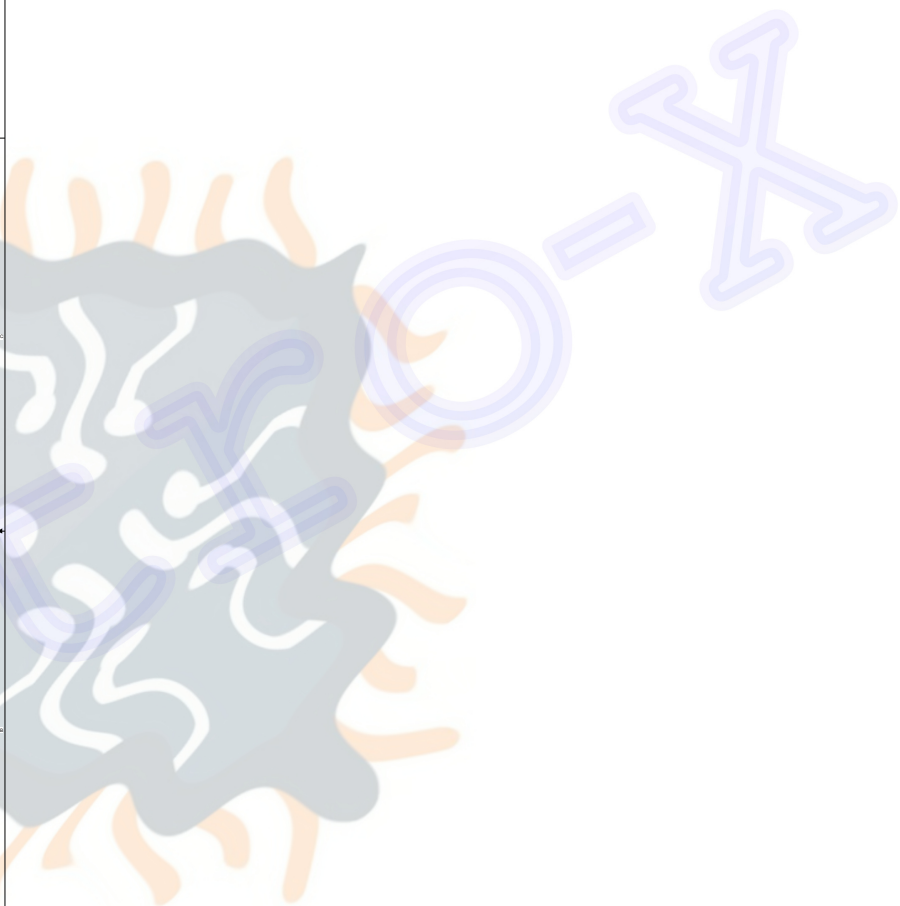




Version change list
(P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Modified schematic-15U_09-22C for 15W series.		1. Added charger discharge MOSFET PQ60. 2. Changed the EMI input cap of CPU core to SF000004M00. 3. Reserved DCIN MOSFET PQ102.	2014/09/23	DB0
2	Fine tune Vcore compensation	67	1. Change PR120 from 1.4k ohm to 1.69k ohm 2. Change PC110 from 1000pF to 3300pF 3. Change PC116 from 0.015uF to 8200pF 4. Change PR127 from 28.7k ohm to 48.7k ohm 5. Change PR145 from 22.6k ohm to 23.2k ohm 6. Change PC131 from 1000pF to 820pF 7. Change PR169 BOM Structure from H42@ to @H42@ 8. Change PR177 BOM Structure to @H42@ 9. Change PR164 from 75k ohm to 80.6k ohm 10. Change PR166 from 75k ohm to 80.6k ohm 11. Change PR189 BOM Structure to @H42@ 12. Change PC145 BOM Structure to @H42@ 13. Change PR193 BOM Structure from @ to H44e@	2015/01/05	DB1
3	Change Charger Pmon connection as HP request		1. Delete PC454 2. Reserve PR475, 23.2k ohm	2015/03/16	SI1
4	Fine tune Vcore compensation		1. Reserve PC161 & PR369 2. Un-pop PR122 3. Un-pop PR197, PR198, PR199	2015/03/16	SI1
5	HP request		1. On p60, change SLP_S4# to 2.5V_PG at PR53-1 and change PG6OD+1.2VP to 1.2V_PG at PU3-10, and remove PU4, PR91 and PR156. 2. On p61, change KBC_PWR_ON to 1.8VALW_PG at PR410-1, and change PR410 = 0 ohm and Uninstall PC16. 3. On p62, Change PM_RSMRST# to 1.8VALW_PG, and add a 10k-R (pulled up to +3VALW) at PU33-1. 4. On p66, add a 10k-R (pulled up to +3VDS) at PU34-1 for 2.5V_PG.	2015/03/18	SI1
6	1.Change press button force shutdown circuit 2.Update battery detection connection		1.Change PR461 pin1 from +5VL to +5VDS 2.Delete PR364 Add PR24, PR21, PR364	2015/05/08	SI2
7	1. For Pmon setting 2. For thermal request 2. For +1.8V leakage issue		1.Change PR176 from 20k to 40.2k 2.Change PL35 & PL36 to Z=3mm 3.Change PR368 to 4.99k ohm and PR370 to 2.49k ohm	2015/06/03	SI2
8	1. Add GT phase3 compensation		1. Change PR189, PC145, PR177 to H44e@	2015/06/28	PV
9	1. Solve SN2850 Pmon accuracy issue		1. Change PR333, PR334 from 10 ohm to 0 ohm	2015/07/16	PV
10	1. For PU44 2nd source compatibility		1. Change PU44 TP pin from GND to VIN	2015/07/16	PV
11	1. Add Psys function		1. Install PC161 2. Change PR176 from 40.2k ohm to 13k ohm	2015/07/20	PV
12	Change OTP setting		1. Change PR111 from 14.3 kohm to 19.1kohm	2015/07/29	PV
13	Change VR H4+4e Ilim setting		1. Change PR155 from 16.9 kohm to 14.7kohm 2. Change PR151 from 21 kohm to 22.1kohm 3. Change PR175 from 84.5 kohm to 73.2kohm	2015/07/29	PV
14	1). During power up, delay +1.2V (VDDQ) powerup until +2.5V (VPP) is ready.	60	1. Change PR53 from 0 ohm to 100k ohm 2. Add PD10, PD11	2015/09/04	PVR
15	2). During power off, delay +2.5V (VPP) power off later than VDDQ via RC delay.	66	1. Change PR371 from 0 ohm to 100 ohm 2. Add PR6 100k ohm 3. Add PD12 4. Change PR472 from 0.22uF to 0.47uF and instal	2015/09/04	PVR
16	Fine tune power reset RC to meet 11~12 seconds	57	1. Change PR461 from 560k ohm to 1M ohm 2. Add PR462, PR463 931k ohm	2015/09/04	PVR
17	Change 0 ohm to short pad		PR18, PR128, PR132, PR135, PR136, PR139, PR142, PR369, PR159, PR202, PR322, PR333, PR334, PR356, PR357, PR360, PR363, PR411, PR366, PR375	2015/09/04	PVR
18	Fine tune power reset RC to meet 11~12 seconds	58	1. Change PR460 from 680k ohm to 649k ohm 2. Add PR464 34k_0402	2015/09/10	PVR
19	HP request	64	1. Change PR372, PR344 from 10k ohm to 30k ohm	2015/09/10	PVR
20	Fine tune CPU compensation for 4+4e	67	1. Change PR145 from 23.7k ohm to 22.1k ohm 2. Change PR154 from 12.7k ohm to 13.7k ohm 3. Change PR147 from 1k ohm to 549 ohm 4. Change PR179 from 52.3k ohm to 59k ohm	2015/09/14	PVR
21	Fine tune GTX compensation for 4+4e	71	1. Change PR432 from 43k ohm to 27k ohm 2. Change PR444 from 10k ohm to 15.8k ohm	2015/09/14	PVR
22	Fine tune CPU compensation for 4+4e	67	1. Change PR120 from 1.27k ohm to 866 ohm 2. Change PR127 from 48.7k ohm to 63.4k ohm 3. Change PR134 from 34.8k ohm to 24.9k ohm	2015/09/15	PVR
23	Change PQ19 pin2 net name		Change PQ19 pin2 net name from ON/OFFBTN_KBC# to ON/OFFBTN#		MV

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Security Classification	28T10516	Compal Secret Data	20080622	Yes	Compal Electronics, Inc.
Revised Date		Disciplined Date			PWR-PHR
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